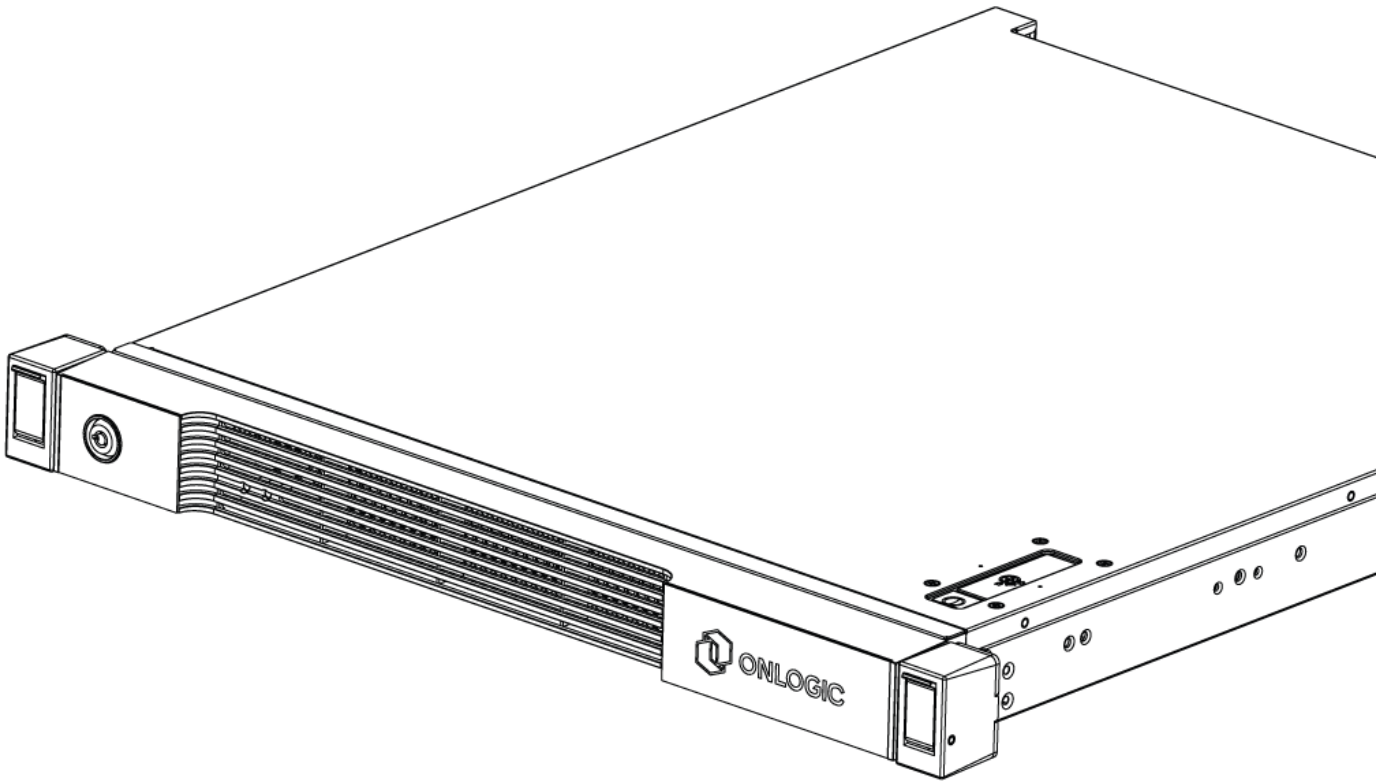
Axial AC101 UEFI Manual



Revision History

Date	Revision History
07/13/2023	First release of Axial AC101 UEFI manual

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

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1.0 - Introduction

This document outlines the UEFI configuration menus and settings for the OnLogic Axial AC101 Edge Server.

Note that within this document, the terms “BIOS” and “UEFI” are often used interchangeably to describe the firmware interface used to start up a system.

UEFI is a more advanced firmware interface which provides similar functionality to legacy BIOS firmware. UEFI provides a more flexible and feature-rich environment for controlling the hardware and boot processes. UEFI is designed to work with larger hard drives and newer hardware features, such as 64-bit processors, Secure Boot, and virtualization.

The Axial AC101 Edge Server leverages modern UEFI firmware for enhanced functionality to enable the most recent technologies.

2.0 - Entering UEFI Setup

To enter the UEFI Setup menu, press the <F2> or <Del> button on a keyboard while the system is powering on.

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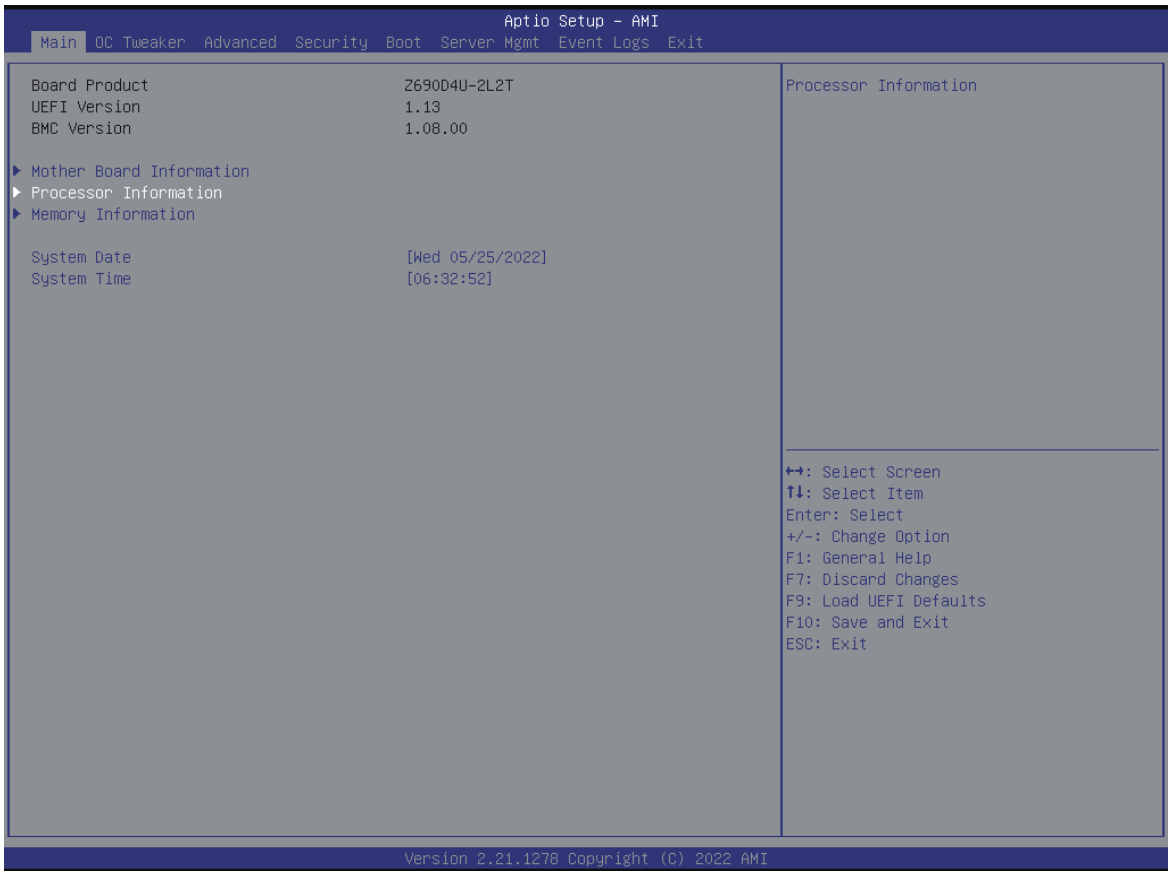
3.0 - Main Screen

Once you enter the UEFI SETUP UTILITY, the Main screen will appear and display the system overview. The Main screen provides system overview information and allows you to set the system time and date.



3.1 - Mother board Information

Enter this item to view the motherboard information.

3.2 - Processor Information

Enter this item to view the processor information.

3.3 - Memory Information

Enter this item to view the memory information.

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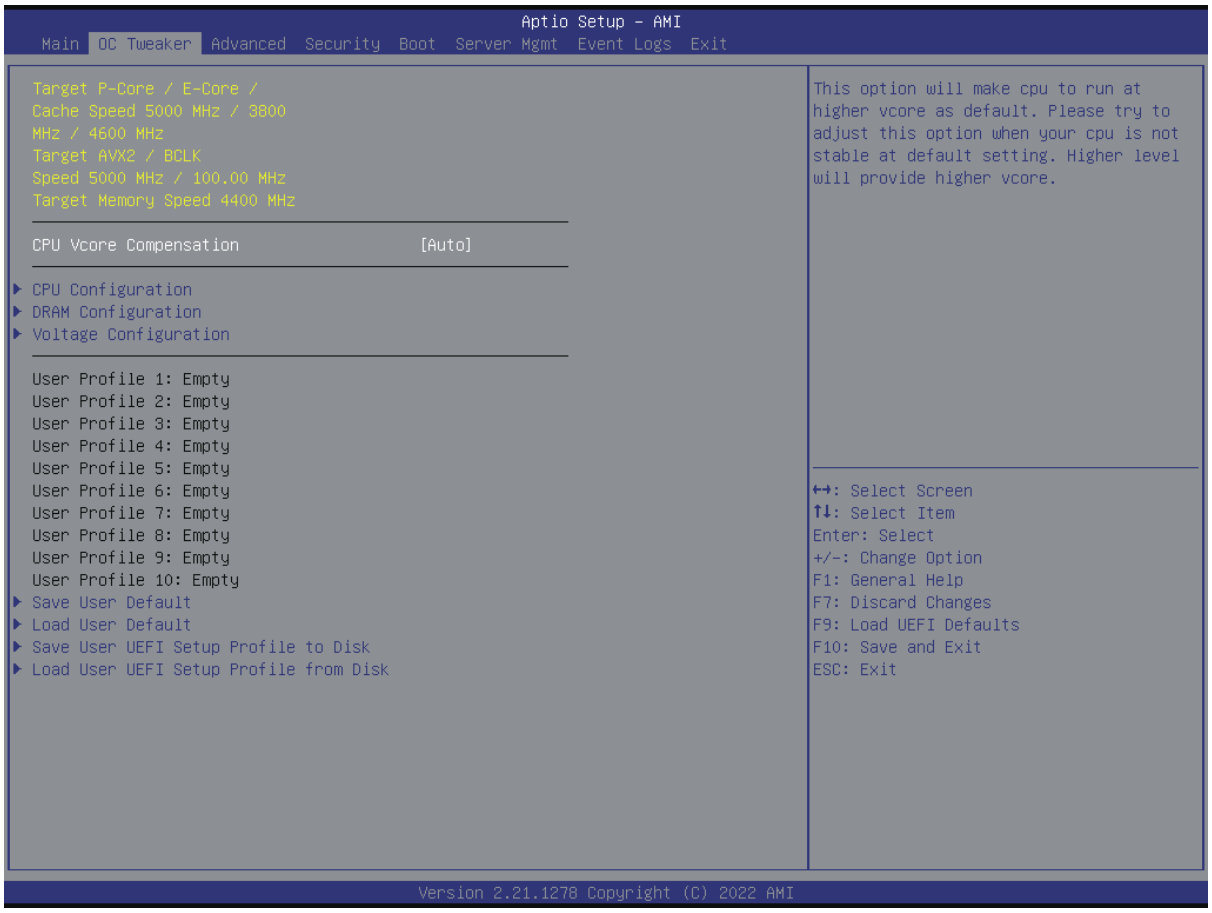
4.0 OC Tweaker



4.1 - CPU Vcore Compensation

This option will make the cpu run at higher Vcores as default. Please try to adjust this option when your cpu is not stable at default setting. Higher level will provide higher Vcore.

4.2 - Save User Default

Type a profile name and press enter to save your settings as user default.

4.3 - Load User Default

Load previously saved user defaults.

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4.4 - Save User UEFI Setup Profile to Disk

It helps you to save current UEFI settings as a user profile to disk.

4.5 - Load User UEFI Setup Profile from Disk

You can load the previous saved profile from the disk.

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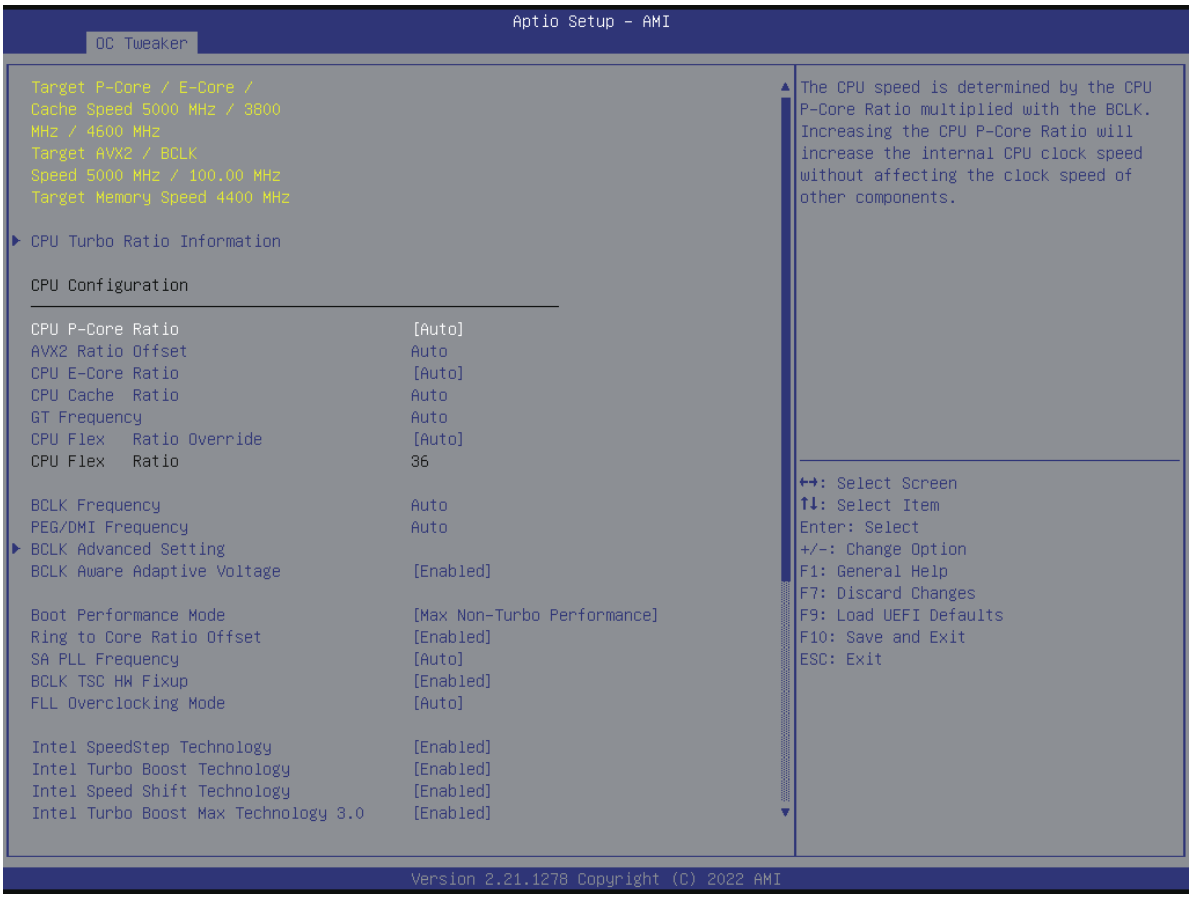
4.6 - CPU Configuration



4.6.1 - CPU Turbo Ratio Information

Allows users to browse the CPU Turbo Ratio Information.

4.6.2 - CPU P-Core Ratio

The CPU speed is determined by the CPU P-Core Ratio multiplied with the BCLK. Increasing the CPU P-Core Ratio will increase the internal CPU clock speed without affecting the clock speed of other components.

4.6.3 - AVX2 Ratio Offset

AVX2 Ratio Offset specifies a negative offset from the CPU Ratio for AVX workloads. AVX is a more stressful workload that lowers the AVX ratio to ensure the maximum possible ratio for SSE workloads.

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4.6.4 - CPU E-Core Ratio

The E-Core speed is determined by the E-Core Ratio multiplied with the BCLK. Increasing the E-Core Ratio will increase the internal E-Core clock speed without affecting the clock speed of other components.

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4.6.5 - CPU Cache Ratio

The CPU Internal Bus Speed Ratio. The maximum should be the same as the CPU Ratio.

4.6.6 - GT Frequency

Configure the frequency of the integrated GPU in MHz.

4.6.7 - CPU Flex Ratio Override

Enable/Disable CPU Flex Ratio Programming. Flex Ratio can lower maximum non- turbo, especially for CPU without turbo function.

4.6.8 - BCLK Frequency

The CPU speed is determined by the CPU Ratio multiplied with the BCLK. Increasing the BCLK will increase the internal CPU clock speed but also affect the clock speed of other components.

4.6.9 - PEG/DMI Frequency

Configure the PEG/DMI Frequency setting.

4.6.10 - BCLK Advanced Setting

Configure the BCLK Advanced setting.

4.6.11 - BCLK SSC Mode

Configure the BCLK Spread Spectrum Mode setting.

4.6.12 - BCLK Delay

After raising BCLK, BIOS adds a delay time (ms) for stability.

4.6.13 - BCLK Aware Adaptive Voltage

BCLK Aware Adaptive Voltage enable/disable. When enabled, pcode will be aware of the BCLK frequency when calculating the CPU V/F curves. This is ideal for BCLK OC to avoid high voltage overrides.

4.6.14 - Boot Performance Mode

Select the performance state that the BIOS will set before OS handoff. Max Battery mode will set CPU ratio as xB till OS handoff. This option is suggested for BCLK overclocking

4.6.15 - Ring to Core Ratio Offset

Disable Ring to Core Ratio Offset so the ring and core can run at the same frequency.

4.6.16 - SA PLL Frequency Override

Configure SA PLL Frequency.

4.6.17 - BCLK TSC HW Fixup

BCLK TSC HW Fixup disabled during TSC copy from PMA to APIC.

4.6.18 - FLL Overclocking Mode

Nominal is good for normal core ratio overclocking. Elevated and Extremely Elevated are good for high BCLK OC.

4.6.19 - Intel SpeedStep Technology

Intel SpeedStep technology allows processors to switch between multiple frequencies and voltage points for better power saving and heat dissipation. CPU turbo ratio can be fixed when Intel SpeedStep Technology set Disabled and Intel Turbo Boost Technology set Enabled.

4.6.20 - Intel Turbo Boost Technology

Intel Turbo Boost Technology enables the processor to run above its base operating frequency when the operating system requests the highest performance state.

4.6.21 - Intel Speed Shift Technology

Enable/Disable Intel Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-States.

For the best support of Intel Turbo Boost Max Technology 3.0 (ITBMT 3.0), enable Intel Speed Shift Technology. If your CPU does not support ITBMT 3.0, the option will be grayed out.

4.6.22 - Intel Turbo Boost Max Technology 3.0

Enable/Disable Intel Turbo Boost Technology 3.0 (ITBMT 3.0) support. Disabling will report the maximum ratio of the slowest core in _CPC object. Processors supporting the ITBMT 3.0 feature contain at least one processor core whose maximum ratio is higher than the others.

4.6.23 - Intel Thermal Velocity Boost Voltage Optimizations

This service controls thermal based voltage optimizations for processors that implement the Intel Thermal Velocity Boost (TVB) feature.

4.6.24 - TVB Information

Enter this item to view TVB information.

4.6.25 - CPU Tj Max

Set CPU Tj Max to adjust TCC Target Temperature. Support TjMax in the range of 62 to 115 deg Celsius.

4.6.26 - Dual Tau Boost

Enable Dual Tau Boost feature for 35W/65W/125W CPU to achieve performance boost with additional PL1 greater than TDP for limited durations

4.6.27 - Load Intel Base Power Limit Settings

Enable/Disable Load Intel Base Power Limit Settings. When enabled, the power limit and current limit will be using Intel Base Power Limit Settings.

4.6.28 - Long Duration Power Limit

Configure Package Power Limit 1 in watts. When the limit is exceeded, the CPU ratio will be lowered after a period of time. A lower limit can protect the CPU and save power, while a higher limit may improve performance.

4.6.29 - Long Duration Maintained

Configure the period of time until the CPU ratio is lowered when the Long Duration Power Limit is exceeded.

4.6.30 - Short Duration Power Limit

Configure Package Power Limit 2 in watts. When the limit is exceeded, the CPU ratio will be lowered immediately. A lower limit can protect the CPU and save power, while a higher limit may improve performance.

4.6.31 - CPU Core Unlimited Current Limit

To unlock the voltage regulator current limit completely, you can set this option to Enabled.

4.6.32 - CPU Core Current Limit

Configure the Voltage Regulator Current Limit. This value represents the Maximum instantaneous current allowed at any given time.

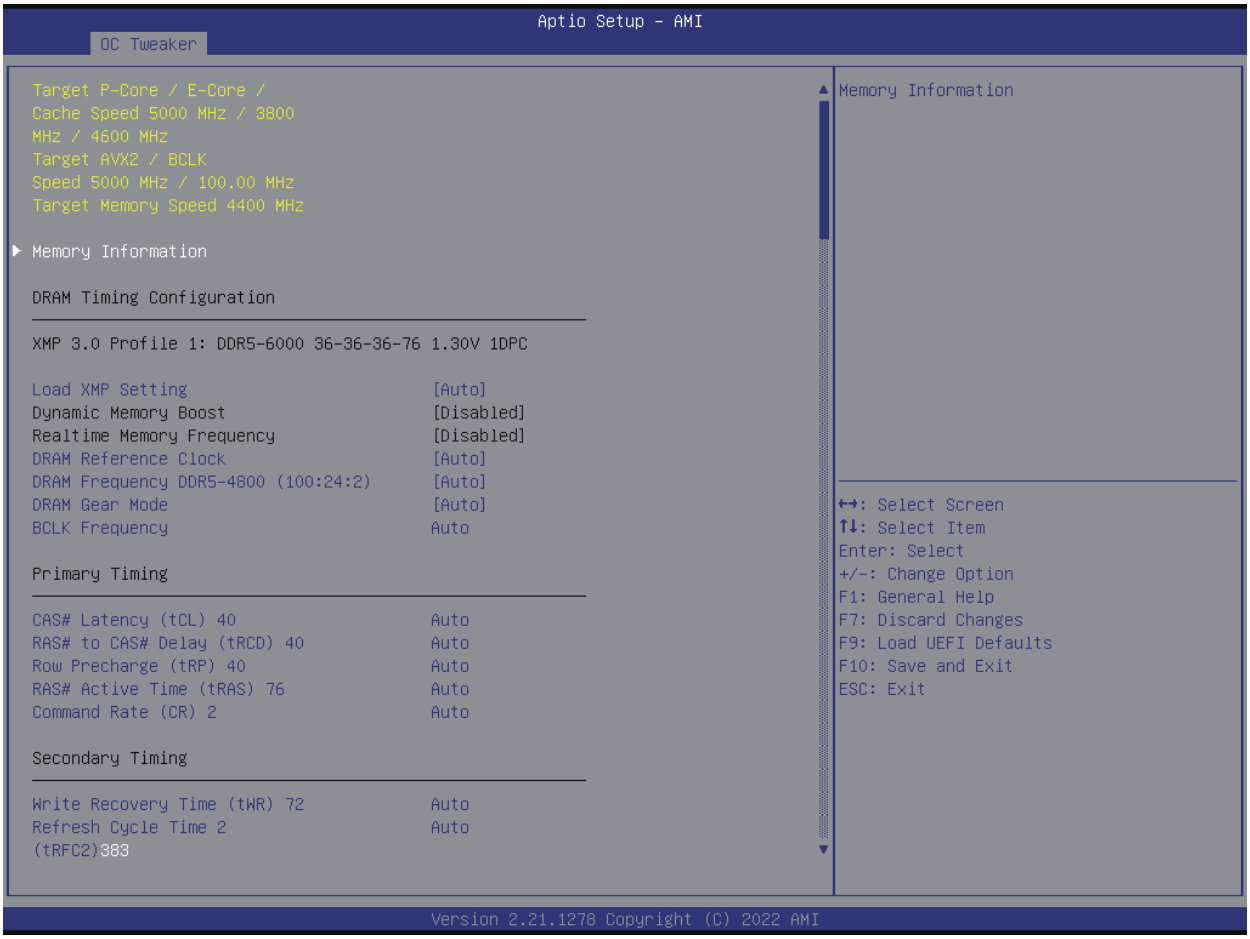
4.6.33 - GT Unlimited Current Limit

To unlock the voltage regulator current limit completely, you can set this option to Enabled.

4.6.34 - GT Current Limit

Configure the Voltage Regulator Current Limit. This value represents the Maximum instantaneous current allowed at any given time.

4.7 - DRAM Configuration



4.7.1 - Memory Information

Allows users to browse the serial presence detect (SPD) and Intel extreme memory profile (XMP) for DDR modules.

4.7.2 - DRAM Timing Configuration

IMPORTANT NOTE: Modification of DRAM Timing settings should only be modified and configured by experts. Only the default (Auto) settings are tested and validated by OnLogic. Improper configuration may impact system functionality and/or stability.

4.7.2.1 - Load XMP Setting

Load XMP settings to overclock the DDR memory and perform beyond standard specifications.

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4.7.2.3 - DRAM Reference Clock

Select Auto for optimized settings.

4.7.2.4 - DRAM Frequency

If [Auto] is selected, the motherboard will detect the memory module(s) inserted and assign the appropriate frequency automatically.

4.7.2.5 - DRAM Gear Mode

High gear is good for high frequency

4.7.2.6 - BCLK Frequency

The CPU speed is determined by the CPU Ratio multiplied with the BCLK. Increasing the BCLK will increase the internal CPU clock speed but also affect the clock speed of other components.

4.7.3 - Primary Timing

4.7.3.1 - CAS# Latency (tCL)

The time between sending a column address to the memory and the beginning of the data in response.

4.7.3.2 - RAS# to CAS# Delay (tRCD)

The number of clock cycles required between the opening of a row of memory and accessing columns within it.

4.7.3.3 - Row Precharge Time (tRP)

The number of clock cycles required between the issuing of the precharge command and opening the next row.

4.7.3.4 - RAS# Active Time (tRAS)

The number of clock cycles required between a bank active command and issuing the precharge command.

4.7.3.5 - Command Rate (CR)

The delay between when a memory chip is selected and when the first active command can be issued.

4.7.4 - Secondary Timing

4.7.4.1 - Write Recovery Time (tWR)

The amount of delay that must elapse after the completion of a valid write operation, before an active bank can be precharged.

4.7.4.2 - Refresh Cycle Time2 (tRFC2)

The number of clocks from a Refresh command until the first Activate command to the same rank.

4.7.4.3 - Refresh Cycle Time per Bank (tRFCpb)

The number of clocks that a per back Refresh command takes to complete.

4.7.4.4 - RAS to RAS Delay (tRRD_L)

The number of clocks between two rows activated in different banks of the same rank.

4.7.4.5 - RAS to RAS Delay (tRRD_S)

The number of clocks between two rows activated in different banks of the same rank.

4.7.4.6 - Write to Read Delay (tWTR_L)

The number of clocks between the last valid write operation and the next read command to the same internal bank.

4.7.4.7 - Write to Read Delay (tWTR_S)

The number of clocks between the last valid write operation and the next read command to the same internal bank.

4.7.4.8 - Read to Precharge (tRTP)

The number of clocks that are inserted between a read command to a row pre- charge command to the same rank.

4.7.4.9 - Four Activate Window (tFAW)

The time window in which four activates are allowed the same rank.

4.7.4.10 - CAS Write Latency (tCWL)

Configure CAS Write Latency.

4.7.4.11 - Third Timing tREFI

Configure refresh cycles at an average periodic interval.

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4.7.4.12 - tCKE

Configure the period of time the DDR5 initiates a minimum of one refresh command internally once it enters Self-Refresh mode.

4.7.4.13 - tRC

Configure the minimum active to active/Refresh Time.

4.7.5 - Turn Around Timing

4.7.5.1 - Turn Around Timing Optimization

Auto is enabled in the general case.

4.7.5.2 - TAT Training Value tRDRD_sg

Configure between module read to read delay.

4.7.5.3- tRDRD_dg

Configure between module read to read delay.

4.7.5.4 - tRDRD_dr

Configure between module read to read delay.

4.7.5.5 - tRDRD_dd

Configure between module read to read delay.

4.7.5.6 - tRDWR_sg

Configure between module read to write delay.

4.7.5.7 - tRDWR_dg

Configure between module read to write delay.

4.7.5.8 - tRDWR_dr

Configure between module read to write delay.

4.7.5.9 - tRDWR_dd

Configure between module read to write delay.

4.7.5.10 - tWRRD_sg

Configure between module write to read delay.

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4.7.5.11 - tWRRD_dg

Configure between module write to read delay.

4.7.5.12 - tWRRD_dr

Configure between module write to read delay.

4.7.5.13 - tWRRD_dd

Configure between module write to read delay.

4.7.5.14 - tWRWR_sg

Configure between module write to write delay.

4.7.5.15 - tWRWR_dg

Configure between module write to write delay.

4.7.5.16 - tWRWR_dr

Configure between module write to write delay.

4.7.5.17 - tWRWR_dd

Configure between module write to write delay.

4.7.5.18 - TAT Runtime Value tRDRD_sg

Minimum delay from read to read to the same bank group in tCK cycles.

4.7.5.19 - tRDRD_dg

Minimum delay from read to read to different bank groups in tCK cycles.

4.7.5.20 - tRDRD_dr

Minimum delay from read to read to the other rank in the same DIMM in tCK cycles.

4.7.5.21 - tRDRD_dd

Minimum delay from read to read to the other DIMM in tCK cycles.

4.7.5.22 - tRDWR_sg

Minimum delay from read to write to the same bank group in tCK cycles.

4.7.5.23 - tRDWR_dg

Minimum delay from read to write to different bank groups in tCK cycles.

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4.7.5.24 - tRDWR_dr

Minimum delay from read to write to the other rank in the same DIMM in tCK cycles.

4.7.5.25 - tRDWR_dd

Minimum delay from read to write to the other DIMM in tCK cycles.

4.7.5.26 - tWRRD_sg

Minimum delay from write to read to the same bank group in tCK cycles.

4.7.5.27 - tWRRD_dg

Minimum delay from write to read to different bank groups in tCK cycles.

4.7.5.28 - tWRRD_dr

Minimum delay from write to read to the other rank in the same DIMM in tCK cycles.

4.7.5.29 - tWRRD_dd

Minimum delay from write to read to the other DIMM in tCK cycles.

4.7.5.30 - tWRWR_sg

Minimum delay from write to write in the same bank group in tCK cycles.

4.7.5.31 - tWRWR_dg

Minimum delay from write to write to different bank groups in tCK cycles.

4.7.5.32 - tWRWR_dr

Minimum delay from write to write to the other rank in the same DIMM in tCK cycle.

4.7.5.33 - tWRWR_dd

Minimum delay from write to write to the other DIMM in tCK cycles.

4.7.6 - Round Trip Timing

4.7.6.1 - Round Trip Timing Optimization

Auto is enabled in the general case.

4.7.6.2 - Round Trip Level

Configure round trip level.

4.7.6.3 - Initial RTL IO Delay Offset

Configure round trip latency IO delay initial offset.

4.7.6.4 - Initial RTL FIF0 Delay Offset

Configure round trip latency FIF0 delay initial offset.

4.7.6.5 - Initial RTL (MC0 C0 A1/A2)

Configure round trip latency initial value.

4.7.6.6 - Initial RTL (MC0 C1 A1/A2)

Configure round trip latency initial value.

4.7.6.7 - Initial RTL (MC1 C0 B1/B2)

Configure round trip latency initial value.

4.7.6.8 - Initial RTL (MC1 C1 B1/B2)

Configure round trip latency initial value.

4.7.6.9 - RTL (MC0 C0 A1/A2)

Configure round trip latency.

4.7.6.10 - RTL (MC0 C1 A1/A2)

Configure round trip latency.

4.7.6.11 - RTL (MC1 C0 B1/B2)

Configure round trip latency.

4.7.6.12 - RTL (MC1 C1 B1/B2)

Configure round trip latency.

4.7.6.13 - Dimm ODT Training

ODT values will be optimized by Dimm On-Die Termination Training.

4.7.6.14 - ODT WR (A1)

Configure the memory on die termination resistors WR.

4.7.6.15 - ODT WR (A2)

Configure the memory on die termination resistors WR.

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4.7.6.16 - ODT WR (B1)

Configure the memory on die termination resistors WR.

4.7.6.17 - ODT WR (B2)

Configure the memory on die termination resistors WR.

4.7.6.18 - ODT NOM Rd (A1)

Configure the memory on die termination resistors NOM Rd.

4.7.6.19 - ODT NOM Rd (A2)

Configure the memory on die termination resistors NOM Rd.

4.7.6.20 - ODT NOM Rd (B1)

Configure the memory on die termination resistors NOM Rd.

4.7.6.21 - ODT NOM Rd (B2)

Configure the memory on die termination resistors NOM Rd.

4.7.6.22 - ODT PARK (A1)

Configure the memory on die termination resistors PARK.

4.7.6.23 - ODT PARK (A2)

Configure the memory on die termination resistors PARK.

4.7.6.24 - ODT PARK (B1)

Configure the memory on die termination resistors PARK.

4.7.6.25 - ODT PARK (B2)

Configure the memory on die termination resistors PARK.

4.7.6.26 - ODT PARK DQS (A1)

Configure the memory on die termination resistors PARK DQS.

4.7.6.27 - ODT PARK DQS (A2)

Configure the memory on die termination resistors PARK DQS.

4.7.6.28 - ODT PARK DQS (B1)

Configure the memory on die termination resistors PARK DQS.

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4.7.6.29 - ODT PARK DQS (B2)

Configure the memory on die termination resistors PARK DQS.

4.7.6.30 - ODT CA (A1 Group A)

Configure the memory on die termination resistors ODT CA.

4.7.6.31 - ODT CA (A2 Group A)

Configure the memory on die termination resistors ODT CA.

4.7.6.32 - ODT CA (B1 Group A)

Configure the memory on die termination resistors ODT CA.

4.7.6.33 - ODT CA (B2 Group A)

Configure the memory on die termination resistors ODT CA.

4.7.6.34 - ODT CA (A1 Group B)

Configure the memory on die termination resistors ODT CA.

4.7.6.35 - ODT CA (A2 Group B)

Configure the memory on die termination resistors ODT CA.

4.7.6.36 - ODT CA (B1 Group B)

Configure the memory on die termination resistors ODT CA.

4.7.6.37 - ODT CA (B2 Group B)

Configure the memory on die termination resistors ODT CA.

4.7.6.38 - ODT CS (A1 Group A)

Configure the memory on die termination resistors ODT CS.

4.7.6.39 - ODT CS (A2 Group A)

Configure the memory on die termination resistors ODT CS.

4.7.6.40 - ODT CS (B1 Group A)

Configure the memory on die termination resistors ODT CS.

4.7.6.41 - ODT CA (B2 Group A)

Configure the memory on die termination resistors ODT CS.

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4.7.6.42 - ODT CS (A1 Group B)

Configure the memory on die termination resistors ODT CS.

4.7.6.43 - ODT CS (A2 Group B)

Configure the memory on die termination resistors ODT CS.

4.7.6.44 - ODT CS (B1 Group B)

Configure the memory on die termination resistors ODT CS.

4.7.6.45 - ODT CS (B2 Group B)

Configure the memory on die termination resistors ODT CS.

4.7.6.46 - ODT CK (A1 Group A)

Configure the memory on die termination resistors ODT CK.

4.7.6.47 - ODT CK (A2 Group A)

Configure the memory on die termination resistors ODT CK.

4.7.6.48 - ODT CK (B1 Group A)

Configure the memory on die termination resistors ODT CK.

4.7.6.49 - ODT CK (B2 Group A)

Configure the memory on die termination resistors ODT CK.

4.7.6.50 - ODT CK (A1 Group B)

Configure the memory on die termination resistors ODT CK.

4.7.6.51 - ODT CK (A2 Group B)

Configure the memory on die termination resistors ODT CK.

4.7.6.52 - ODT CK (B1 Group B)

Configure the memory on die termination resistors ODT CK.

4.7.6.53 - ODT CK (B2 Group B)

Configure the memory on die termination resistors ODT CK.

4.7.7 - Advanced Setting

4.7.7.1 - OnLogic Timing Optimization

Enable/Disable OnLogic Timing Optimization. When Enabled, the memory timing will use OnLogic optimized value.

4.7.7.2 - OnLogic DRAM Frequency Optimization

Enable/Disable OnLogic DRAM Frequency Optimization. When Enabled, the DRAM Frequency will use OnLogic optimized procedure.

4.7.7.3 - MRC Training Respond Time

Configure the MRC Training Respond Time.

4.7.8 - Realtime Memory Timing

4.7.8.1 - Configure the realtime memory timings.

[Enabled] The system will allow performing realtime memory timing changes after MRC_DONE.

4.7.8.2 - Reset for MRC Failed

Reset system after MRC training is failed.

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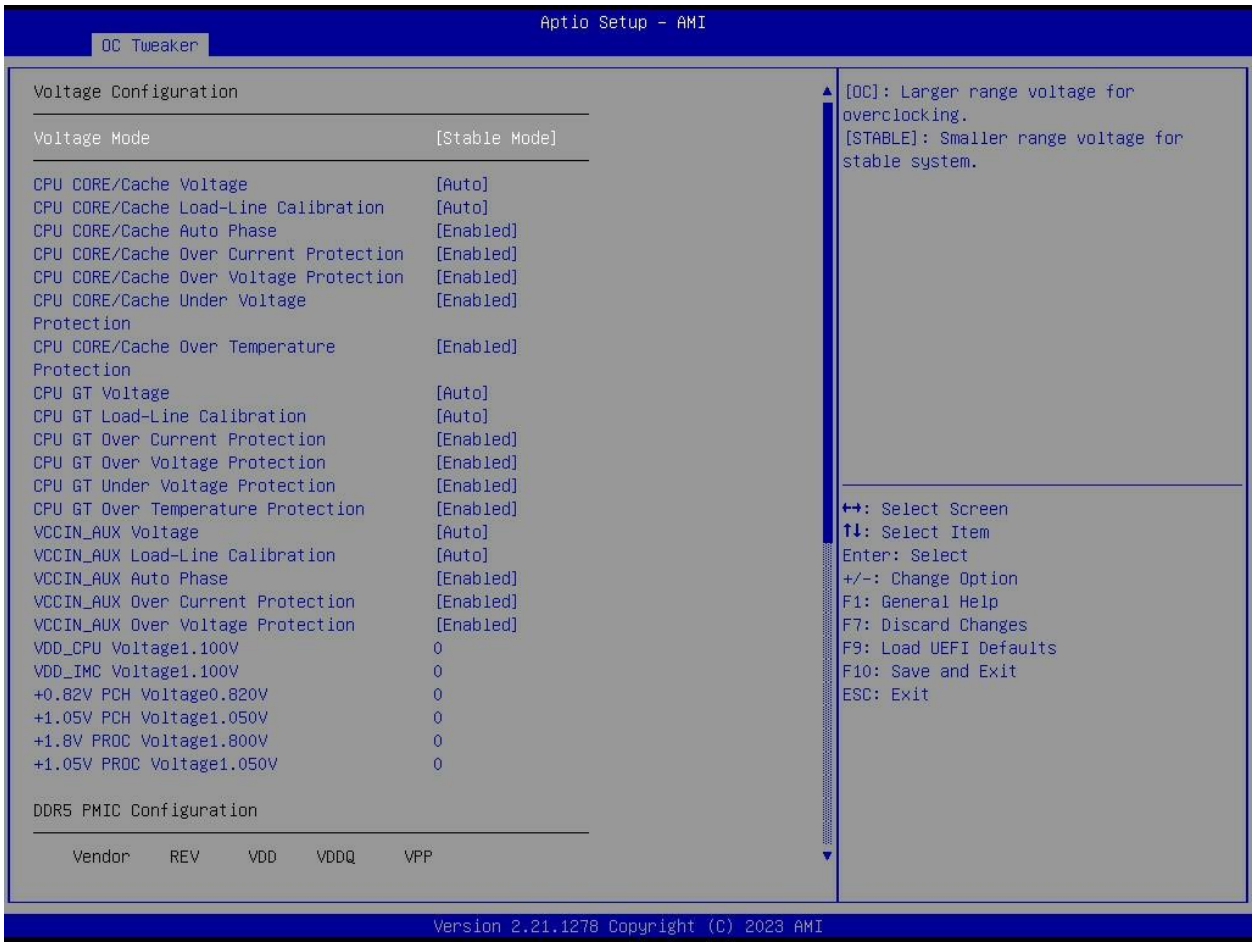
4.8 - Voltage Configuration



IMPORTANT NOTE: Modification of Voltage settings should only be modified and configured by experts. Only the default (Auto) settings are tested and validated by OnLogic. Improper configuration may impact system functionality and/or stability.

4.8.1 - CPU Core/Cache Voltage

Input voltage for the processor by the external voltage regulator.

4.8.2 - CPU Core/Cache Load-Line Calibration

CPU Core/Cache Load-Line Calibration helps prevent CPU Core/Cache voltage droop when the system is under heavy loading.

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4.8.3 - CPU Core/Cache Auto Phase

Configure CPU CORE/Cache Auto Phase

4.8.4 - CPU CORE/Cache Over Current Protection

Configure CPU CORE/Cache Over Current Protection

4.8.5 - CPU CORE/Cache Over Voltage Protection

Configure CPU CORE/Cache Over Voltage Protection.

4.8.6 - CPU CORE/Cache Under Voltage Protection

Configure CPU CORE/Cache Under Voltage Protection.

4.8.7 - CPU CORE/Cache Over Temperature Protection

Configure CPU CORE/Cache Over Temperature Protection.

4.8.8 - CPU GT Voltage

Configure the voltage for the integrated GPU.

4.8.9 - CPU GT Load-Line Calibration

GT Load-Line Calibration helps prevent integrated GPU voltage droop when the system is under heavy load.

4.8.10 - GPU GT Over Current Protection

Configure CPU GT Over Current Protection.

4.8.11 - GPU GT Over Voltage Protection

Configure CPU GT Over Voltage Protection.

4.8.12 - GPU GT Under Voltage Protection

Configure CPU GT Under Voltage Protection.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

4.8.13 - GPU GT Over Temperature Protection

Configure CPU GT Over Temperature Protection.

4.8.14 - VCCIN_AUX Voltage

Input voltage for the processor by the external voltage regulator.

4.8.15 - VCCIN_AUX Load-Line Calibration

VCCIN_AUX Load-Line Calibration helps prevent VCCIN_AUX voltage droop when the system is under heavy loading.

4.8.16 - VCCIN_AUX Phase

Configure VCCIN_AUX Auto Phase

4.8.17 - VCCIN_AUX Over Current Protection

Configure VCCIN_AUX Over Current Protection

4.8.18 - VCCIN_AUX Over Voltage Protection

Configure VCCIN_AUX Over Voltage Protection.

4.8.19 - VCCIN_AUX OTP Mode

Configure VCCIN_AUX OTP Mode

4.8.20 - VCCIN_AUX OTP Temperature

Configure VCCIN_AUX OTP Temperature

4.8.21 - VDD_CPU Voltage

Configure the voltage for the VDD_CPU.

4.8.22 - +0.82V PCH Voltage

Configure the voltage for the +0.82V PCH.

4.8.23 - +1.05 PCH Voltage

Configure the voltage for the +1.05 PCH.

4.8.24 - +1.8V PROC Voltage

Configure the voltage for the +1.8V PROC.

4.8.25 - +1.05V PROC Voltage

Configure the voltage for the +1.05V PROC.

4.8.26 - DRR5 PMIC Configuration PMIC Voltage Option

Choose separate to individually adjust DIMM PMIC.

4.8.27 - VDD Voltage

Configure the memory VDD Voltage

4.8.28 - VDD Voltage Range

Configure the memory VDD Voltage Range.

4.8.29 - VDDQ Voltage

Configure the memory VDDQ Voltage

4.8.30 - VDDQ Voltage Range

Configure the memory VDDQ Voltage Range.

4.8.31 - VPP Voltage

Configure the memory VPP Voltage

4.8.32 - VDD Eventual Voltage

Configure the memory VDD Eventual Voltage

4.8.33 - VDDQ Eventual Voltage

Configure the memory VDDQ Eventual Voltage

4.8.34 - VPP Eventual Voltage

Configure the memory VPP Eventual Voltage

4.8.35 - PMIC Protection Unlock

Configure the PMIC Protection Unclock setting.

4.8.36 - PLL Voltage Configuration P-Core PLL Voltage offset

PLL Voltage offset ranges from 0 to 15 bins, each bin is 15mV. Adding 5 or more bins will help to increase the range of this domain frequency in extreme overclocking conditions. The best bins will be different on each processor, user has to find the best bins for your own processor.

4.8.37 - E-Core PLL Voltage offset

PLL Voltage offset ranges from 0 to 15 bins, each bin is 15mV. Adding 5 or more bins will help to increase the range of this domain frequency in extreme overclocking conditions. The best bins will be different on each processor, user has to find the best bins for your own processor.

4.8.38 - Ring PLL Voltage offset

PLL Voltage offset ranges from 0 to 15 bins, each bin is 15mV. Adding 5 or more bins will help to increase the range of this domain frequency in extreme overclocking conditions. The best bins will be different on each processor, user has to find the best bins for your own processor.

4.8.39 - System Agent PLL Voltage offset

PLL Voltage offset ranges from 0 to 15 bins, each bin is 15mV. Adding 5 or more bins will help to increase the range of this domain frequency in extreme overclocking conditions. The best bins will be different on each processor, user has to find the best bins for your own processor.

4.8.40 - Memory Controller PLL Voltage offset

PLL Voltage offset ranges from 0 to 15 bins, each bin is 15mV. Adding 5 or more bins will help to increase the range of this domain frequency in extreme overclock- ing conditions. The best bins will be different on each processor, user has to find the best bins for your own processor.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

4.8.41 - GT PLL Voltage offset

PLL Voltage offset ranges from 0 to 15 bins, each bin is 15mV. Adding 5 or more bins will help to increase the range of this domain frequency in extreme overclock- ing conditions. The best bins will be different on each processor, user has to find the best bins for your own processor.

4.8.42 - AVX Configuration

4.8.42.1 - AVX2 Voltage Guardband Scale Factor

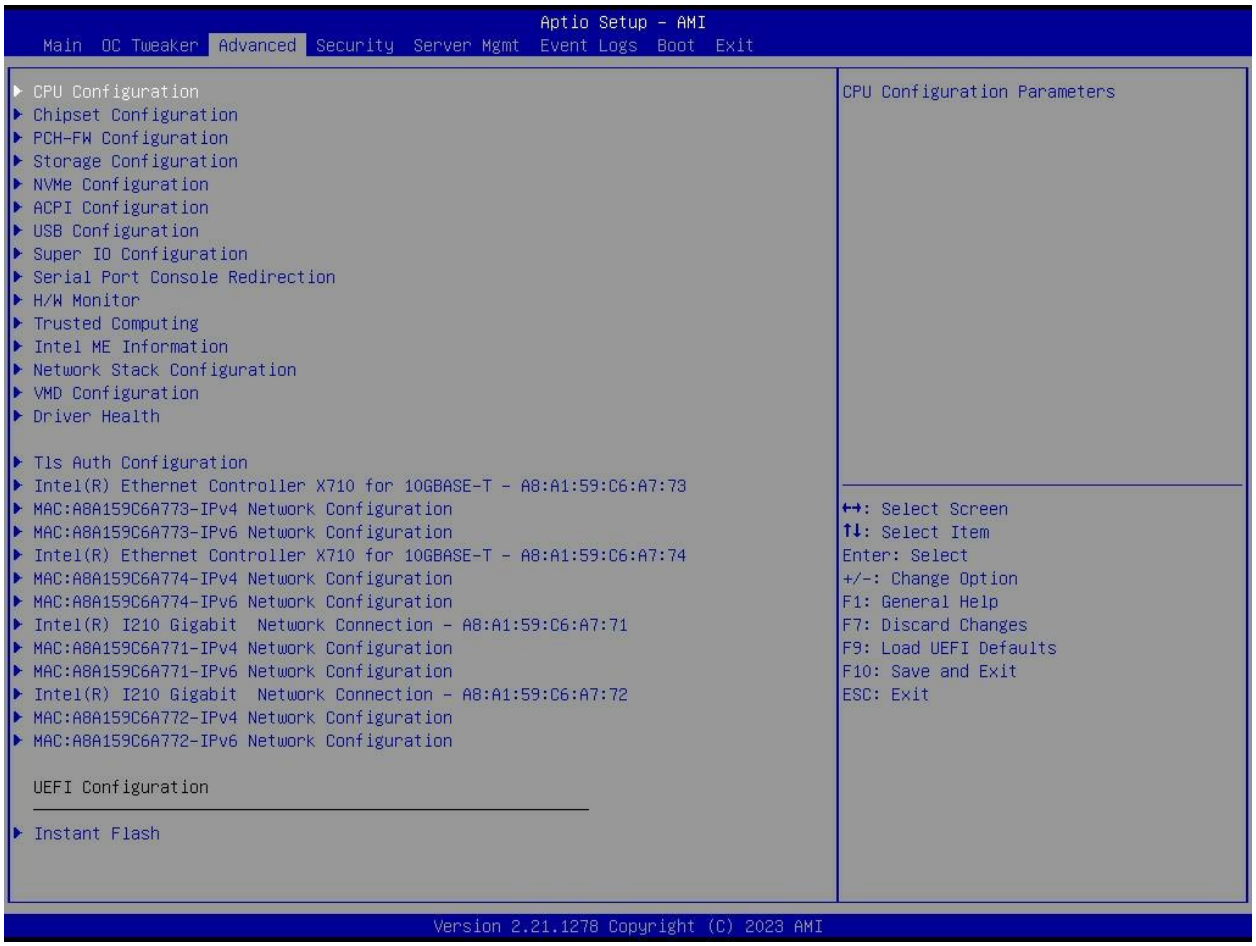
AVX2 Voltage Guardband Scale Factor controls the voltage guardband applied to AVX2 workloads. A value > 1.00 will increase the voltage guardband, and < 1.00 will decrease the voltage guardband

5.0 Advanced Screen

The Advanced configuration screen allows for configuration of the following:

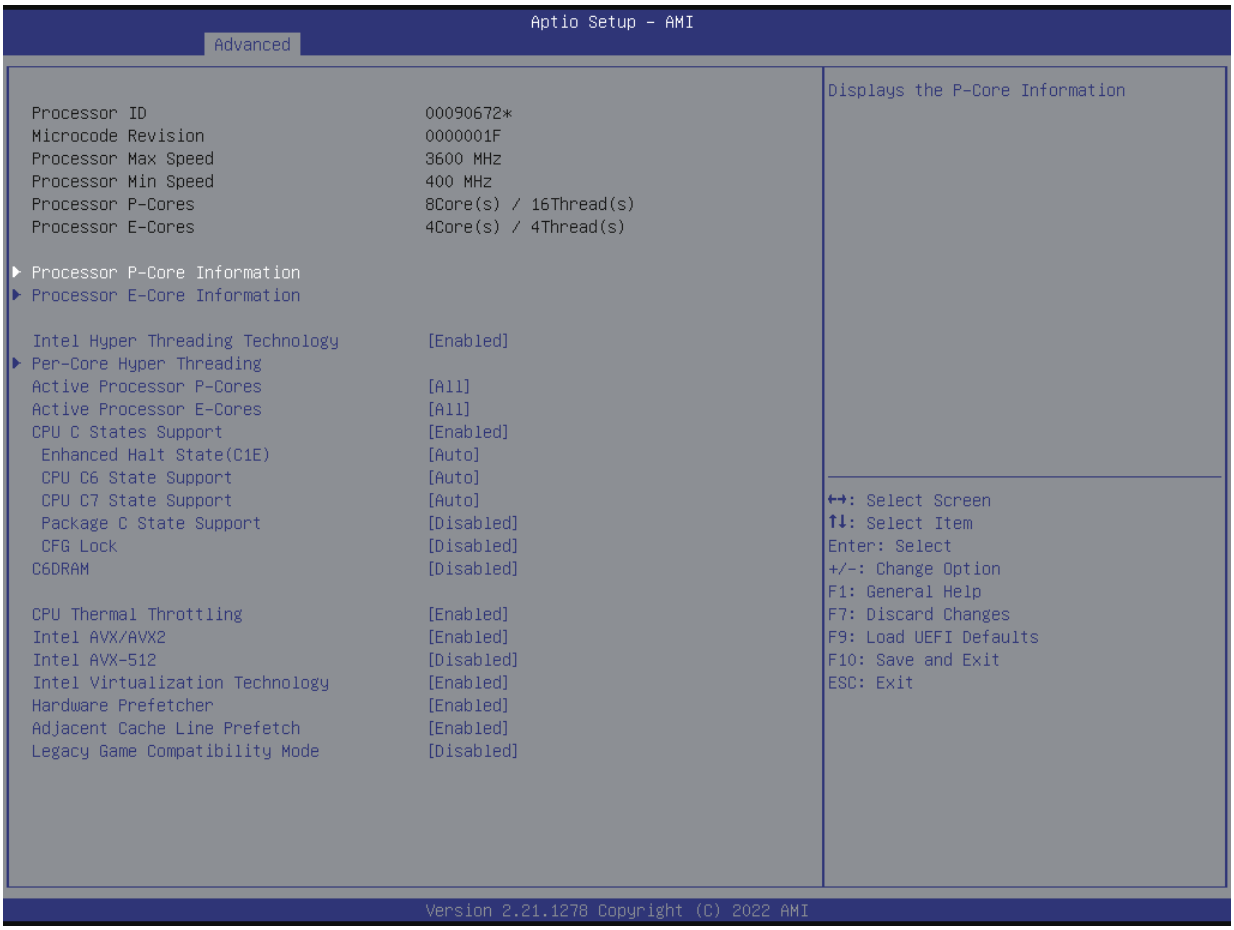
- CPU Configuration
- Chipset Configuration
- PCH-FW Configuration
- Storage Configuration
- NVMe Configuration
- ACPI Configuration
- USB Configuration
- Super IO Configuration
- Serial Port Console Redirection
- H/W Monitor
- Trusted Computing
- Intel ME Configuration
- Network Stack Configuration
- VMD Configuration
- Driver Health
- Instant Flash

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.



Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.1 - CPU Configuration



5.1.1 - Processor P-Core Information

This item displays the P-Core Information.

5.1.2 - Processor E-Core Information

This item displays the E-Core Information.

5.1.3 - Intel Hyper Threading Technology

Intel Hyper Threading Technology allows multiple threads to run on each core, so that the overall performance on threaded software is improved.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.1.4 - Pre-Core Hyper Threading

The Pre-Core Hyper Threading feature allows you to disable Hyper Threading on specific cores.

5.1.5 - Active Processor P-Cores

Select the number of cores to enable in each processor package.

5.1.6 - Active Processor E-Cores

Select the number of E-Cores to enable in each processor package.

5.1.7 - CPU C States Support

Enable CPU C States Support for power saving. It is recommended to keep C6 and C7 enabled for better power saving.

5.1.8 - Enhanced Halt State (C1E)

Enable Enhanced Halt State (C1E) for lower power consumption.

5.1.9 - CPU C6 State Support

Enable C6 deep sleep state for lower power consumption.

5.1.10 - CPU C7 State Support

Enable C7 deep sleep state for lower power consumption.

5.1.11 - Package C State Support

Enable CPU, PCIe, Memory, Graphics C State Support for power saving.

5.1.12 - CFG Lock

This item allows you to disable or enable the CFG Lock.

5.1.13 - C6DRAM

Enable/Disable moving of DRAM contents to PRM memory when CPU is in C6 state.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.1.14 - CPU Thermal Throttling

Enable CPU internal thermal control mechanisms to keep the CPU from overheating.

5.1.15 - Intel AVX/AVX2

Enable/Disable the Intel AVX and AVX2 Instructions. This is applicable for Big Core only.

5.1.16 - Intel AVX-512

Enable/Disable the Intel AVX-512 (a.k.a. AVX3) Instructions. This is applicable for Performance Core only.

5.1.17 - Intel Virtualization Technology

Intel Virtualization Technology allows a platform to run multiple operating systems and applications in independent partitions, so that one computer system can function as multiple virtual systems.

5.1.18 - Hardware Prefetcher

Automatically prefetch data and code for the processor. Enable for better performance.

5.1.19 - Adjacent Cache Line Prefetch

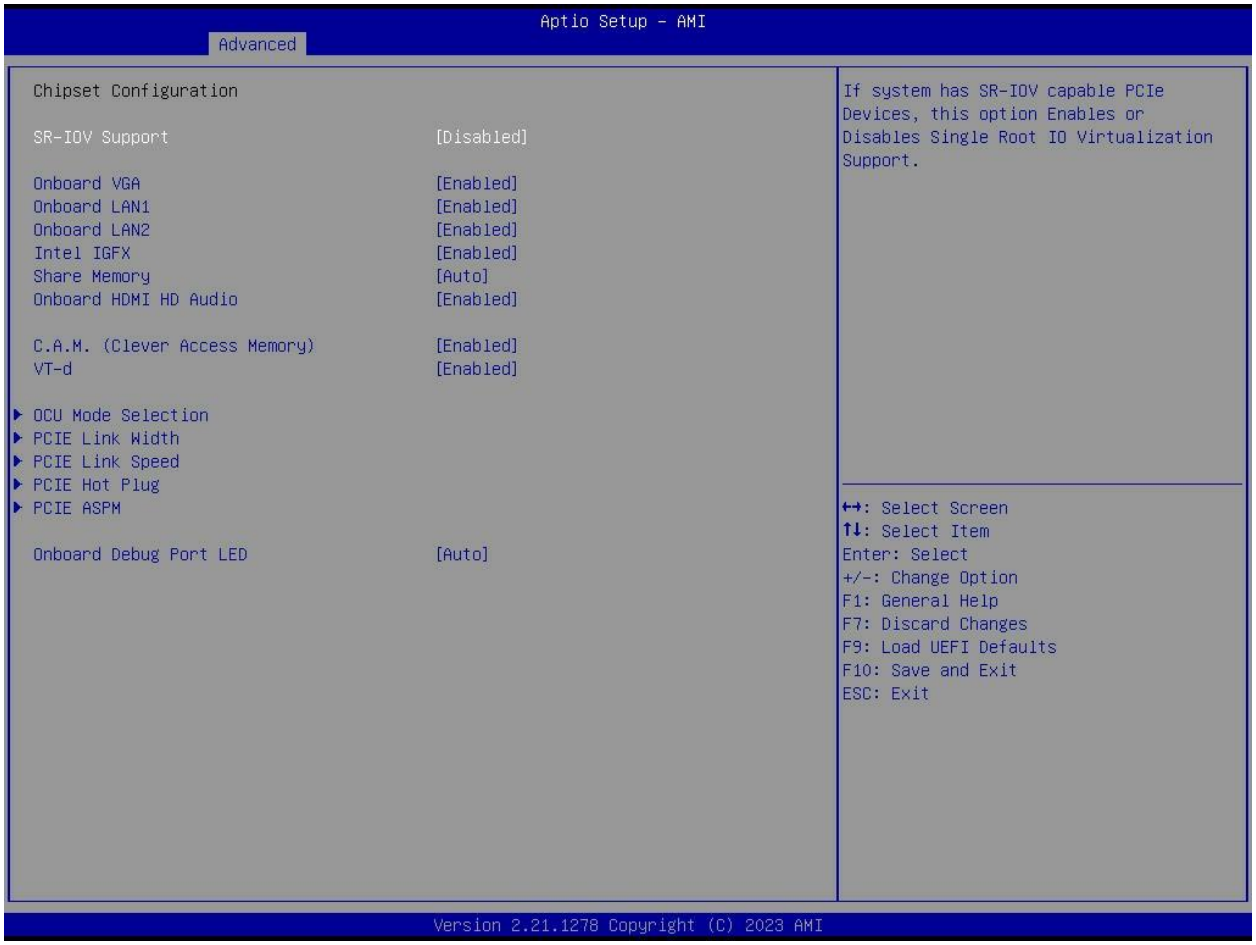
Automatically prefetch the subsequent cache line while retrieving the currently requested cache line. Enable for better performance.

5.1.20 - Legacy Game Compatibility Mode

When enabled, pressing the scroll lock key will toggle the Efficient cores between being parked when Scroll Lock LED is on and un-parked when LED is off.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.2 - Chipset Configuration



5.2.1 - Onboard VGA

To enable or Disable Onboard VGA.

5.2.3 - Onboard LAN1

To enable or Disable Onboard LAN.

5.2.4 - Onboard LAN2

To enable or Disable Onboard LAN.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.2.5 - Intel IGFX

Select to disable the integrated graphics when an external graphics card is installed. Select enable to keep the integrated graphics enabled at all times.

5.2.6 - Share Memory

Configure the size of memory that is allocated to the integrated graphics processor when the system boots up.

5.2.7 - Onboard HDMI HD Audio

Enable audio for the onboard digital outputs.

5.2.8 - C.A.M (Clever Access Memory)

Use this option to enable or disable Resizable BAR support (only if the system supports 64 bit PCI decoding).

5.2.9 - VT-d

Intel® Virtualization Technology for Directed I/O helps your virtual machine monitor better utilize hardware by improving application compatibility and reliability, and providing additional levels of manageability, security, isolation, and I/O performance.

5.2.10 - OCU1 Mode Selection

Switch the COUlink to PCIE/SATA.

5.2.11 - PCIE Link Width

Configure PCIE6 Slot Link Width.

5.2.12 - PCIE Link Speed

Configure PCIE7/OCU4, PCIe6, M.2, PCIe4, OCU1, OCU2, OCU3 Link Speed.

5.2.13 - PCIE Hot Plug Speed

Configure PCIE7/OCU4, PCIe6, M.2, PCIe4, OCU1, OCU2, OCU3 Hot Plug.

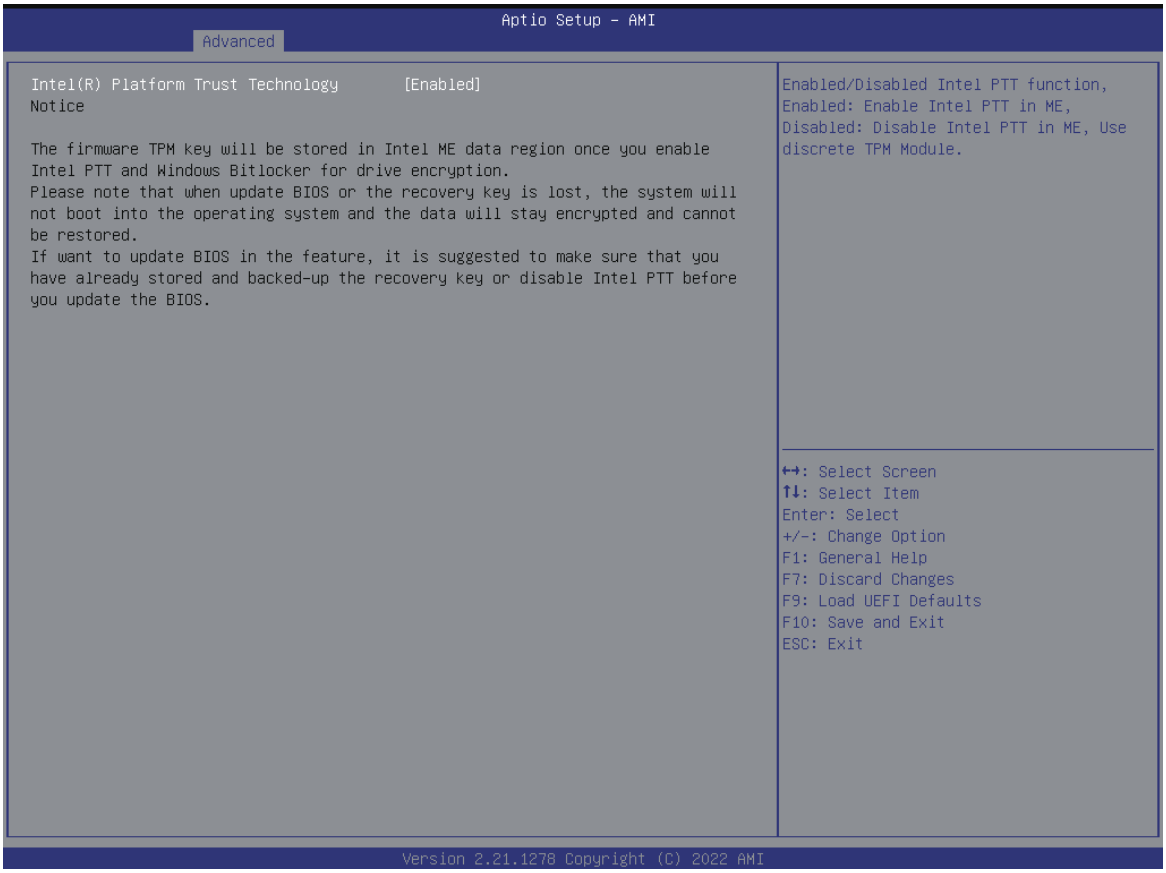
Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.2.14 - PCIE ASPM Support

Configure PCIE7/OCU4, PCIe6, M.2, PCIe4, OCU1, OCU2, OCU3 Hot Plug.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.3 - PCH-FW Configuration

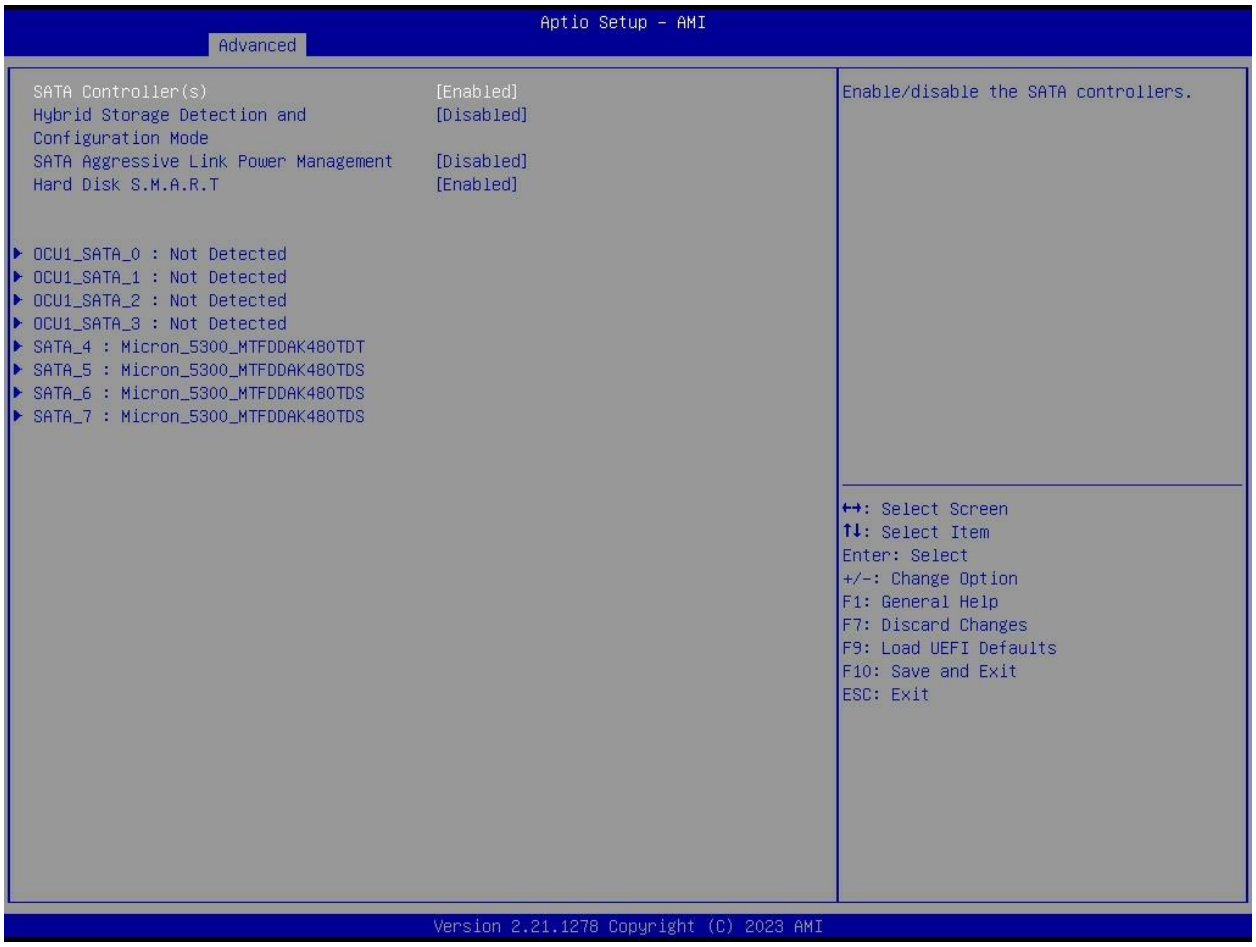


5.3.1 - Intel(R) Platform Trust Technology

Enable/disable Intel PTT in ME. Disable this option to use a discrete TPM Module.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.4 - Storage Configuration



5.4.1 - SATA Controller(s)

Enable/disable the SATA controllers.

5.4.2 - Hybrid Storage Detection and Configuration Mode

This item allows selection of Hybrid Storage Detection and Configuration Mode.

5.4.3 - SATA Aggressive Link Power Management

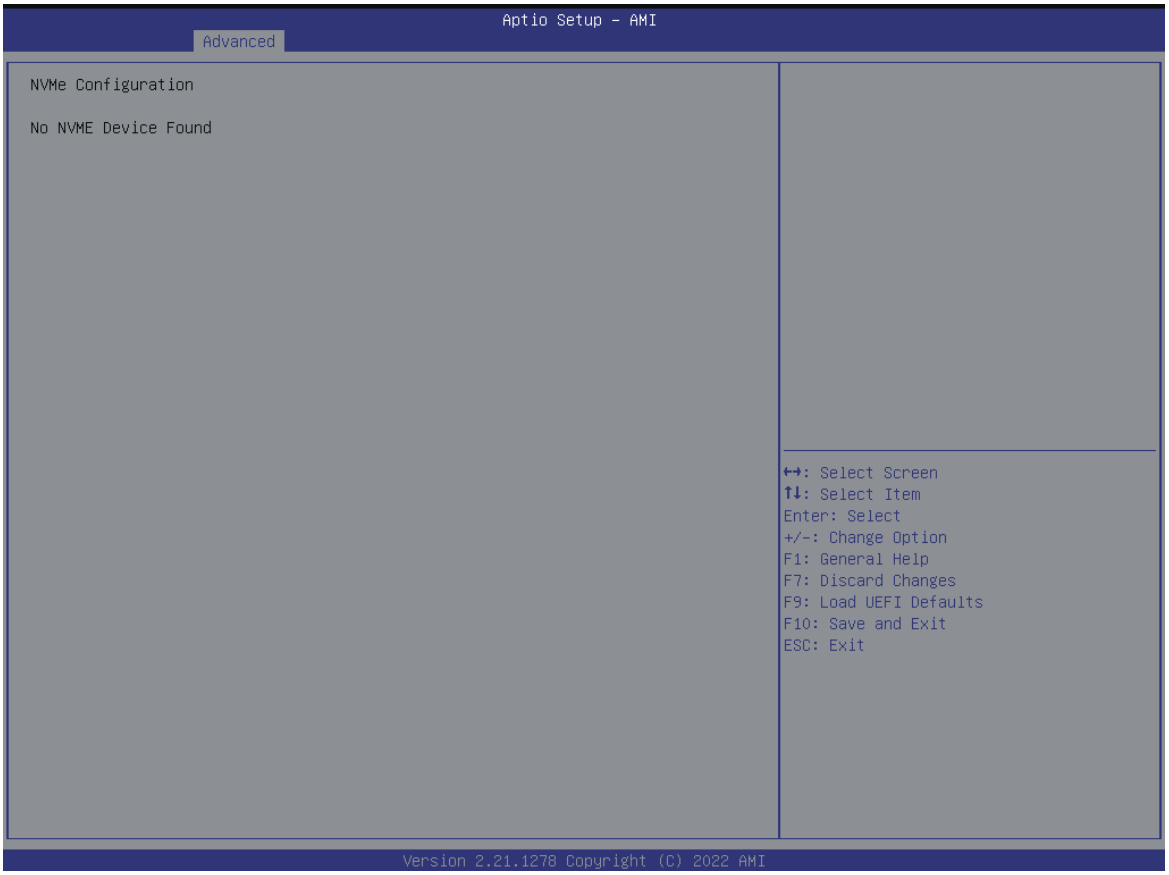
SATA Aggressive Link Power Management allows SATA devices to enter a low power state during periods of inactivity to save power. It is only supported by AHCI mode.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.4.4 - Hard Disk S.M.A.R.T.

S.M.A.R.T stands for Self-Monitoring, Analysis, and Reporting Technology. It is a monitoring system for computer hard disk drives to detect and report on various indicators of reliability.

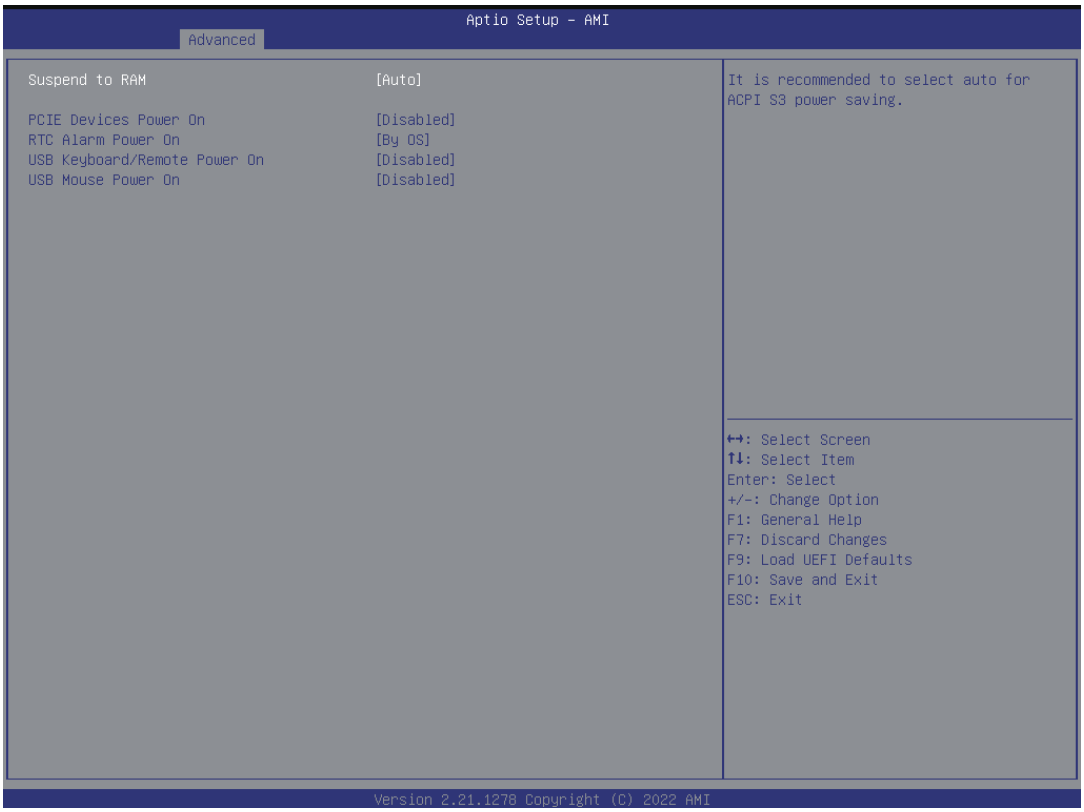
5.5 - NVME Configuration



The NVMe Configuration screen displays the NVMe controller and Drive information.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.6 - ACPI Configuration



5.6.1 - Suspend to RAM

Select disable for ACPI suspend type S1. It is recommended to select auto for ACPI S3 power saving.

5.6.2 - PCIE Devices Power On

Allow the system to be woken up by a PCIE device and enable wake on LAN.

5.6.3 - RTC Alarm Power On

Allow the system to be woken up by the real time clock alarm. Set it to By OS to let it be handled by your operating system.

5.6.4 - USB Keyboard/Remote Power On

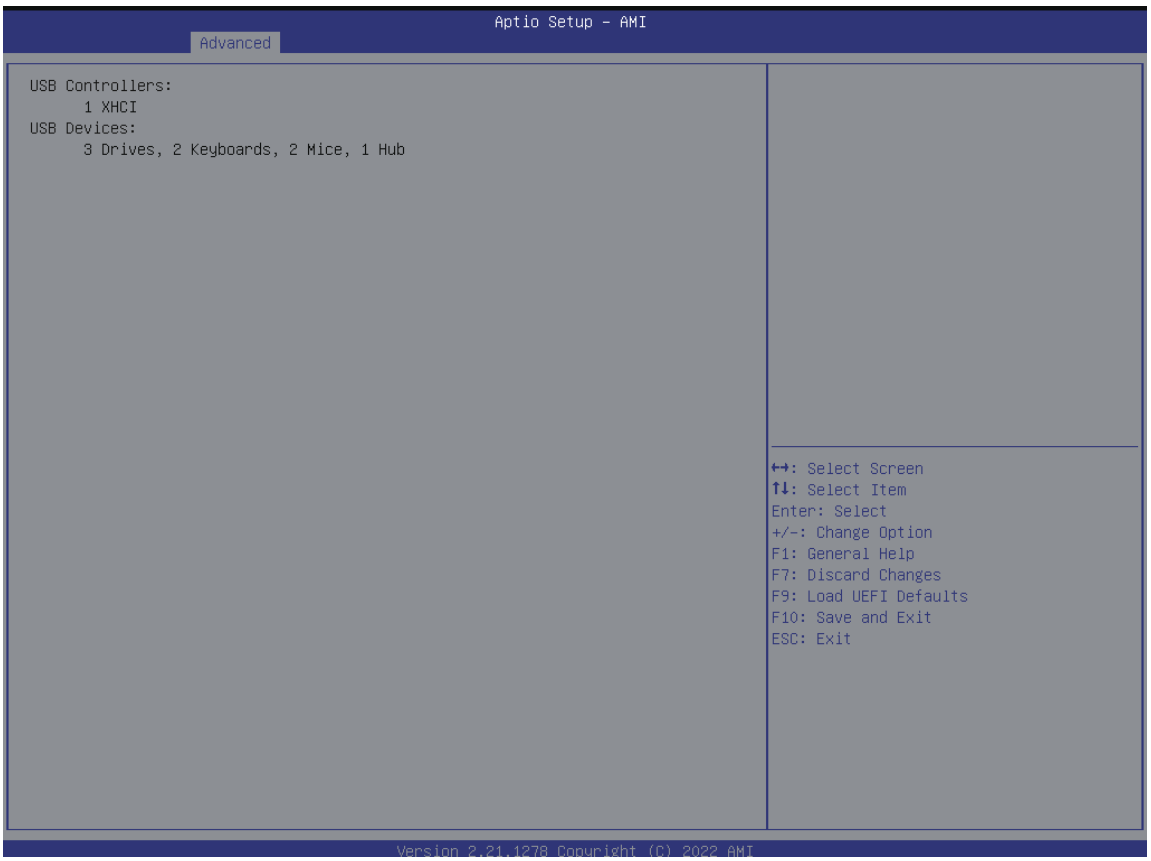
Allow the system to be woken up by an USB keyboard or remote controller.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.6.5 - USB Mouse Power On

Allow the system to be woken up by an USB mouse.

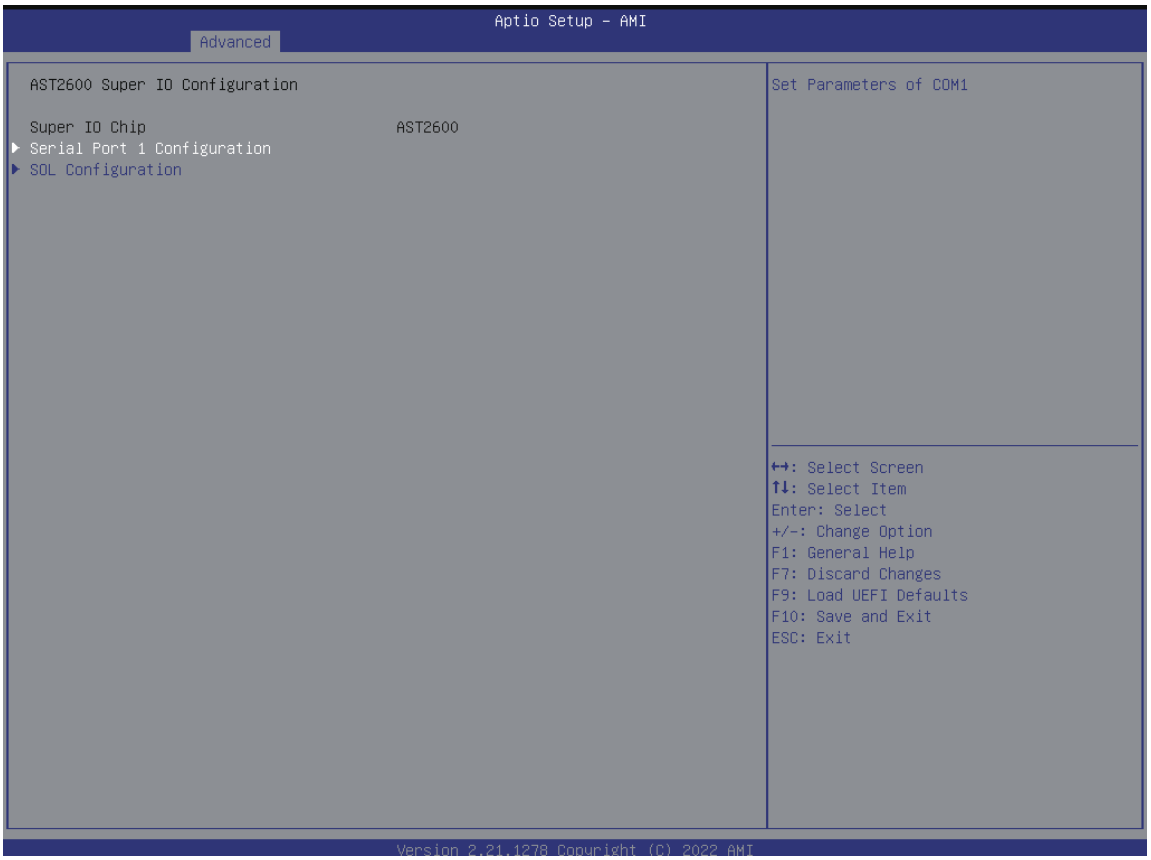
5.7 - USB Configuration



This page displays the information of the USB controllers and USB devices.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.8 - Super IO Configuration



5.8.1 - Serial Port 1 Configuration / SOL Configuration

Use this item to set parameters of COM.

5.8.1.1 - Serial Port

Use this item to enable or disable the serial port (COM).

5.8.1.2 - Change Settings

Use this item to select an optimal setting for a Super IO device.

5.8.2 - SOL Port 1 Configuration

Use this item to set parameters of SOL.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

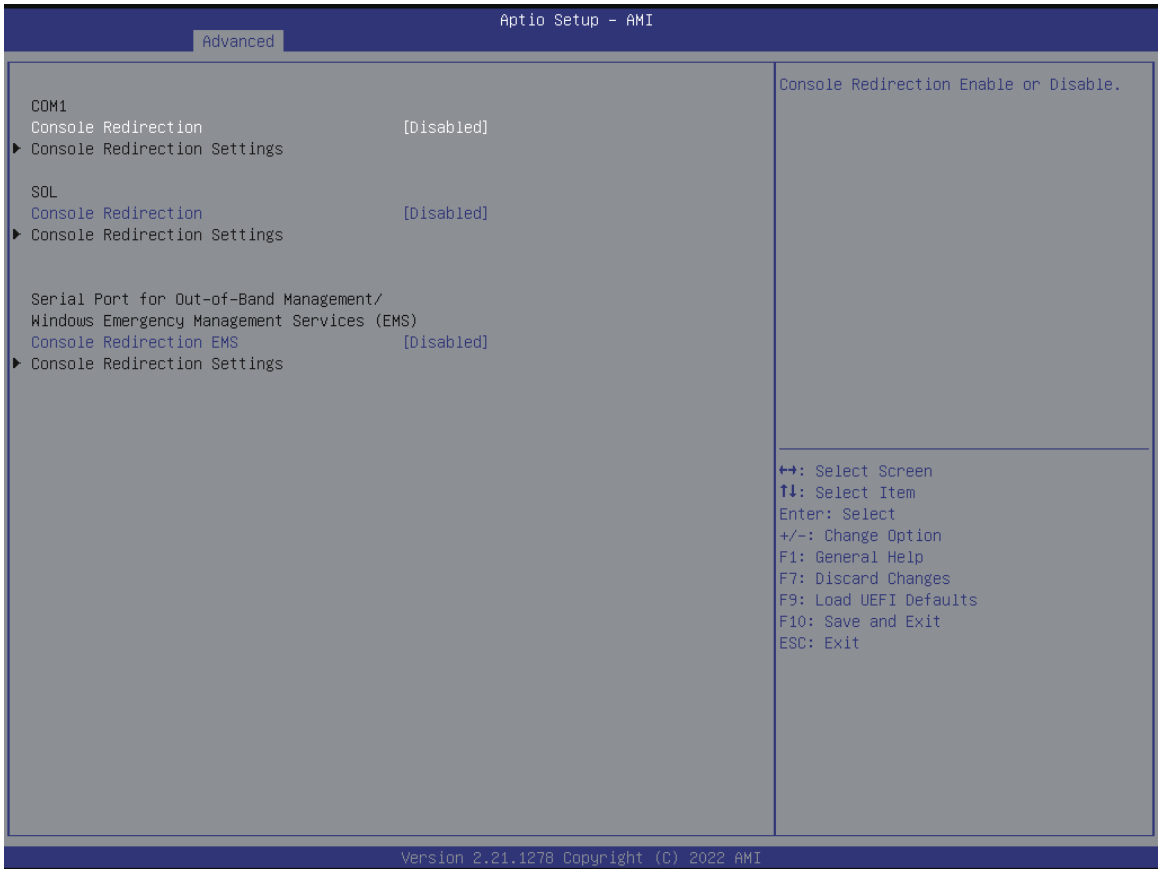
5.8.2.1 - Serial Port

Use this item to enable or disable the SOL port.

5.8.2.2 - Change Settings

Use this item to select an optimal setting for Super IO device.

5.9 - Serial Port Console Redirection



5.9.1 - COM1 / SOL

5.9.1.1 - Console Redirection

Use this option to enable or disable Console Redirection. If this item is set to Enabled, you can select a COM Port to be used for Console Redirection.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.9.1.2 - Console Redirection Settings

Use this option to configure Console Redirection Settings, and specify how your computer and the host computer to which you are connected exchange information.

5.9.1.2.1 - Terminal Type

Use this item to select the preferred terminal emulation type for out-of-band management. It is recommended to select [VT-UTF8].

Option	Description
VT100	ASCII character set
VT100+	Extended VT100 that supports color and function keys
VT-UTF8	UTF8 encoding is used to map Unicode chars onto 1 or more bytes
ANSI	Extended ASCII character set

5.9.1.2.2 - Bits Per Second

Use this item to select the serial port transmission speed. The speed used in the host computer and the client computer must be the same. Long or noisy lines may require lower transmission speed. The options include [9600], [19200], [38400], [57600] and [115200].

5.9.1.2.3 - Data Bits

Use this item to set the data transmission size. The options include [7] and [8] (Bits).

5.9.1.2.4 - Parity

Use this item to select the parity bit. The options include [None], [Even], [Odd], [Mark] and [Space]. A parity bit can be sent with the data bits to detect some transmission errors.Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.

Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd.

Mark: parity bit is always 1. Space: Parity bit is always 0.

5.9.1.2.5 - Stop Bits

The item indicates the end of a serial data packet. The standard setting is [1] Stop Bit. Select

[2] Stop Bits for slower devices.

5.9.1.2.6 - Flow Control

Use this item to set the flow control to prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a "stop" signal can be sent to stop the data flow. Once the buffers are empty, a "start" signal can be sent to restart the flow. Hardware flow uses two wires to send start/stop signals. The options include [None] and [Hardware RTS/CTS].

5.9.1.2.7 - VT-UTF8 Combo Key Support

Use this item to enable or disable the VT-UTF8 Combo Key Support for ANSI/VT100 terminals.

5.9.1.2.8 - Recorder Mode

Use this item to enable or disable Recorder Mode to capture terminal data and send it as text messages.

5.9.1.2.9 - Resolution 100x31

Use this item to enable or disable extended terminal resolution support.

5.9.1.2.10 - Putty Keypad

Use this item to select Function Key and Keypad on Putty.

Legacy Console Redirection

Use this option to configure Legacy Console Redirection Settings, and specify how your computer and the host computer to which you are connected exchange information.

5.9.1.2.11 - Redirection COM Port

Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages.

5.9.1.2.12 - Resolution

On Legacy OS, the Number of Rows and Columns supported redirection.

5.9.1.2.13 - Redirection After BIOS POST

If the [LoadBooster] is selected, legacy console redirection is disabled before booting to legacy OS. If [Always Enabled] is selected, legacy console redirection is enabled for legacy OS. The default value is [Always Enabled].

5.9.2 - Serial Port for Out-of-Band Management/Windows Emergency Management Services (EMS)

5.9.2.1 - Console Redirection

Use this option to enable or disable Console Redirection. If this item is set to Enabled, you can select a COM Port to be used for Console Redirection.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.9.2.2 - Console Redirection Settings

Use this option to configure Console Redirection Settings, and specify how your computer and the host computer to which you are connected exchange information.

5.9.1.2.1 - Out-of-Band Mgmt Port

Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.

5.9.1.2.2 - Terminal Type EMS

Use this item to select the preferred terminal emulation type for out-of-band management. It is recommended to select [VT-UTF8].

Option	Description
VT100	ASCII character set
VT100+	Extended VT100 that supports color and function keys
VT-UTF8	UTF8 encoding is used to map Unicode chars onto 1 or more bytes
ANSI	Extended ASCII character set

5.9.1.2.3 - Bits Per Second EMS

Use this item to select the serial port transmission speed. The speed used in the host computer and the client computer must be the same. Long or noisy lines may require lower transmission speed. The options include [9600], [19200], [57600] and [115200].

5.9.1.2.4 - Flow Control EMS

Use this item to set the flow control to prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a "stop" signal can be sent to stop the data flow. Once the buffers are empty, a "start" signal can be sent to restart the flow. Hardware flow uses two wires to send start/stop signals. The options include [None], [Hardware RTS/ CTS], and [Software Xon/Xoff].

5.9.1.3 - Data Bits EMS

Statically set to 8

5.9.1.4 - Parity EMS

Statically set to None

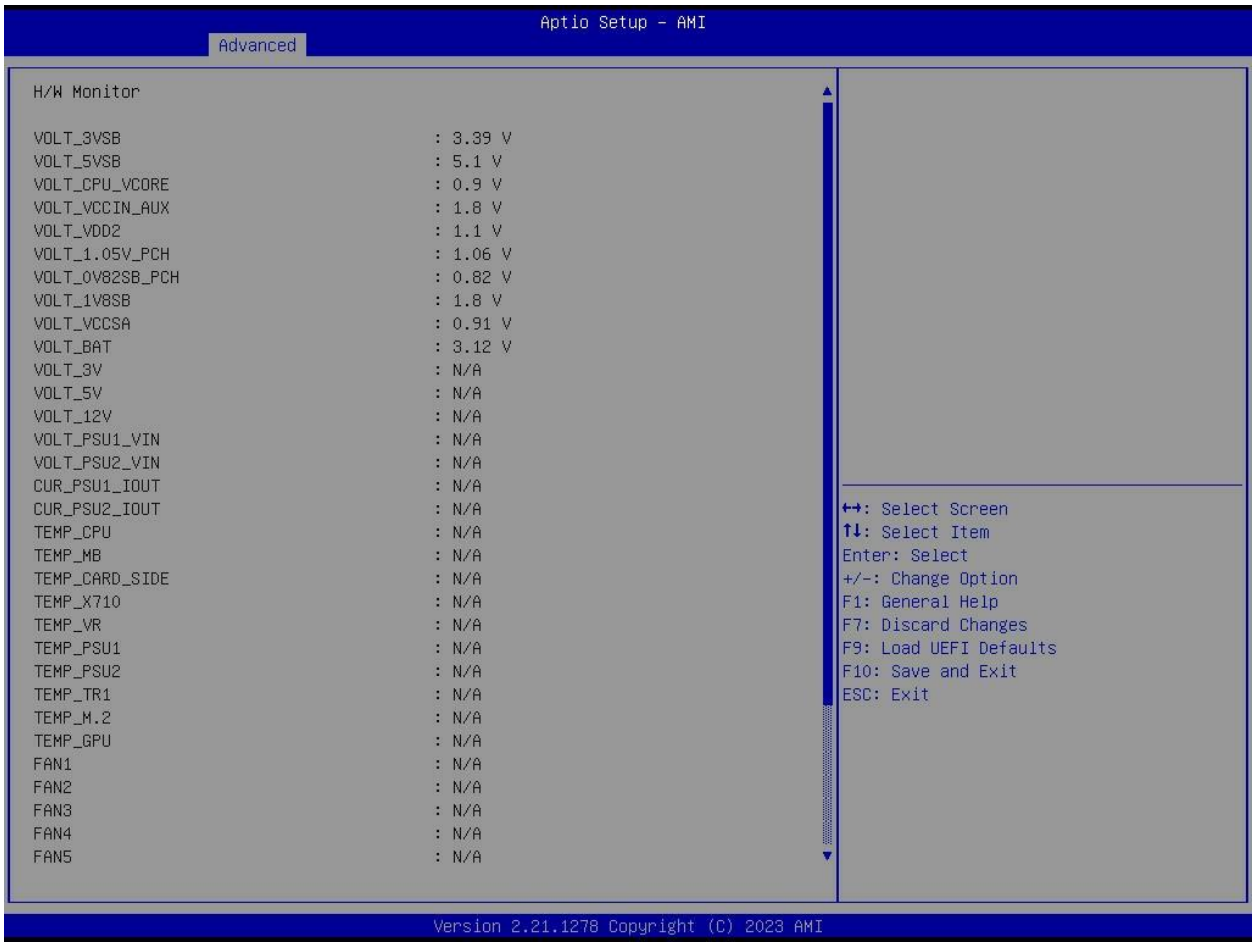
5.9.1.5 - Stop Bits EMS

Statically set to 1

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

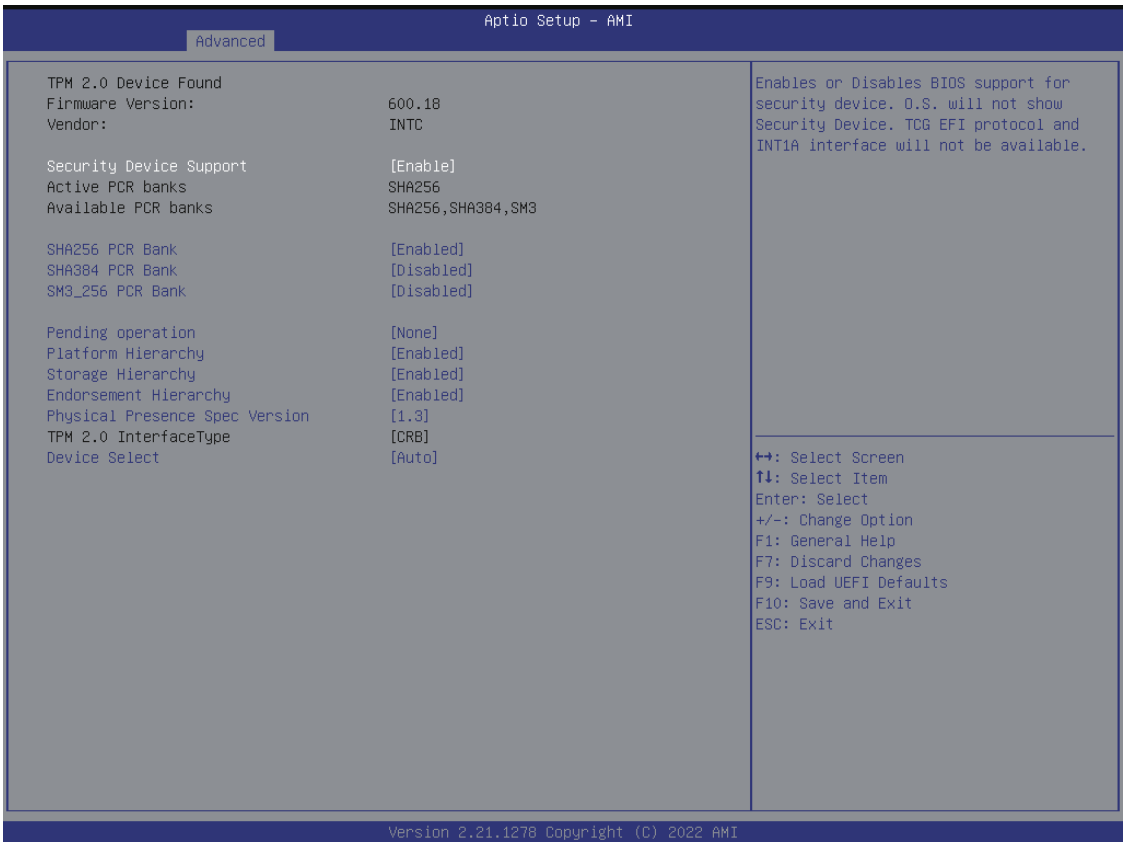
5.10 - H/W Monitor

Monitor the status of the hardware on your system, including the parameters of the CPU temperature, motherboard temperature, CPU fan speed, chassis fan speed, and the critical voltage.



Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.11 - Trusted Computing



5.11.1 - Security Device Support

Enable to activate Trusted Platform Module (TPM) security for your hard disk drives.

5.11.2 - Active PCR banks

This item displays active PCR Banks.

5.11.3 - Available PCR Banks

This item displays available PCR Banks.

5.11.4 - SHA256 PCR Bank

Use this item to enable or disable SHA256 PCR Bank

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.11.5 - SHA384 PCR Bank

Use this item to enable or disable SHA384 PCR Bank.

5.11.6 - SM3_256 PCR Bank

Use this item to enable or disable SM3_256 PCR Bank.

5.11.7 - Pending Operation

Schedule an Operation for the Security Device.

NOTE: Your computer will reboot during restart in order to change the State of the Device.

5.11.8 - Platform Hierarchy

Use this item to enable or disable Platform Hierarchy.

5.11.9 - Storage Hierarchy

Use this item to enable or disable Storage Hierarchy.

5.11.10 - Endorsement Hierarchy

Use this item to enable or disable Endorsement Hierarchy.

5.11.11 - Physical Presence Spec version

Select this item to tell OS to support PPI spec version 1.2 or 1.3. Please note that some HCK tests might not support version 1.3.

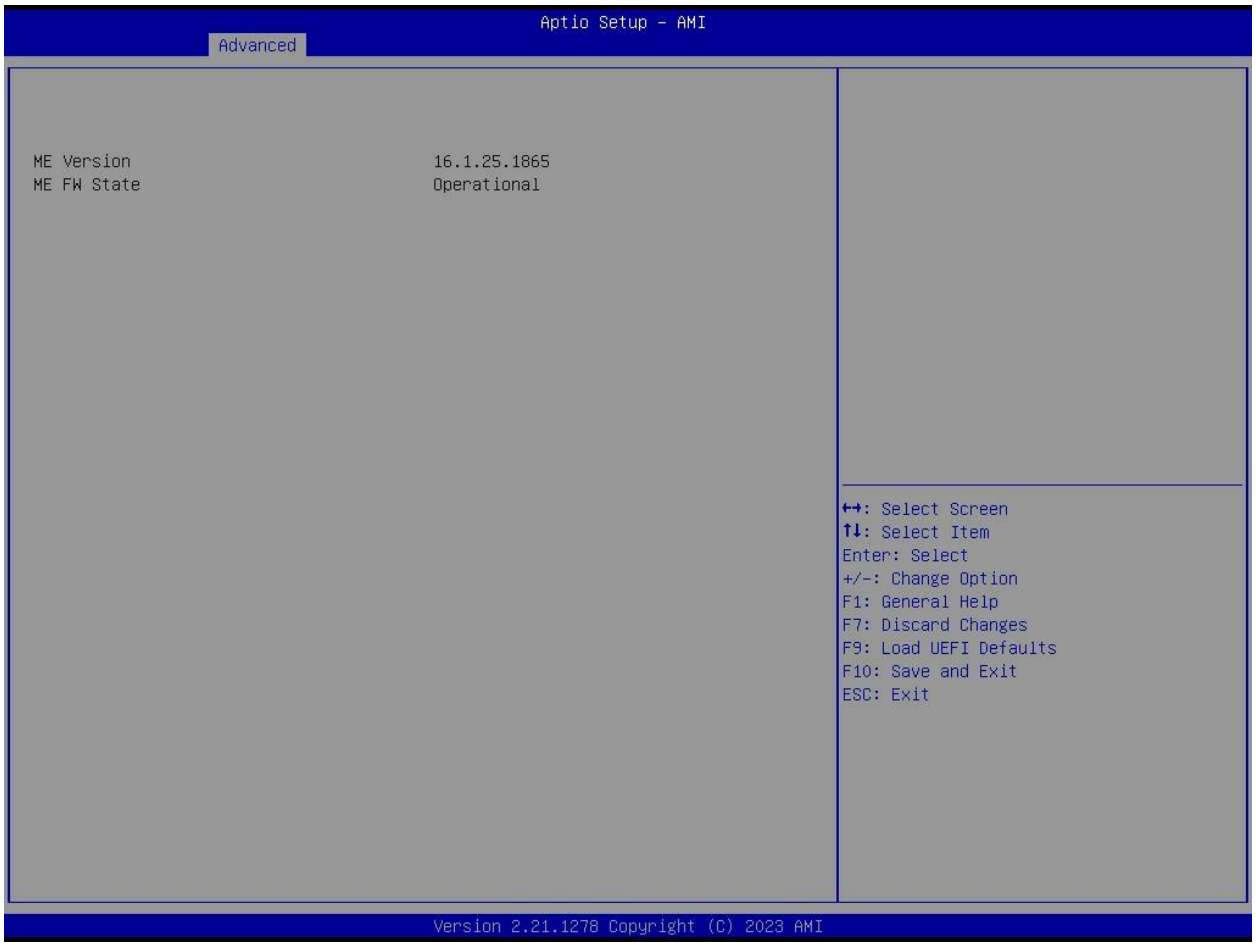
5.11.12 - TPM 2.0 InterfaceType

Select the Communication Interface to TPM 2.0 Device

5.11.13 - Device Select

Use this item to select the TPM device to be supported. TPM 1.2 will restrict support to TPM 1.2 devices. TPM 2.0 will restrict support to TPM 2.0 devices. Auto will support both with the default set to TPM 2.0 devices. If TPM 2.0 devices are not found, TPM 1.2 devices will be enumerated.

5.12 - Intel ME Configuration

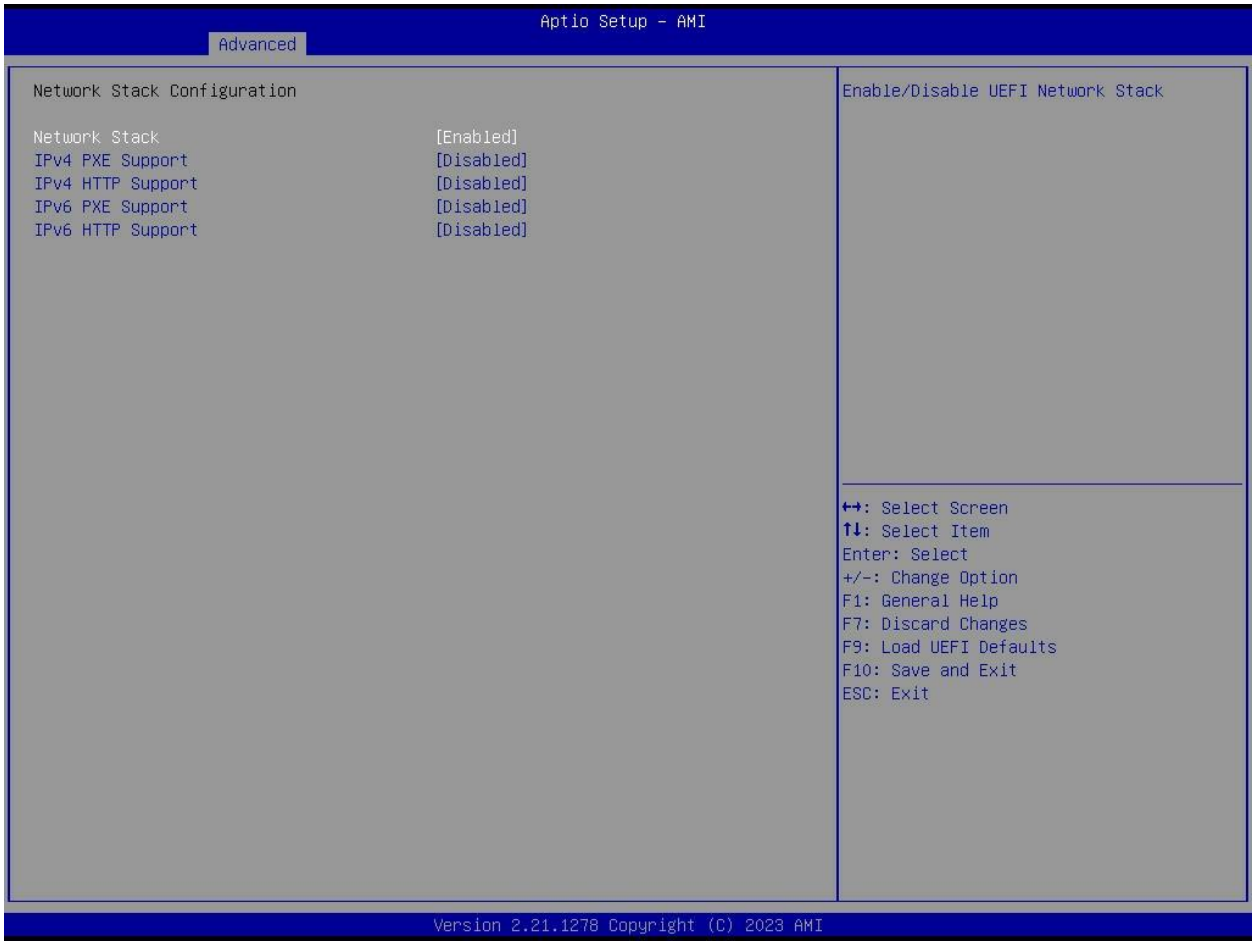


Displays the Intel ME Subsystem Configuration information as follows:

- Operational Firmware Version
- ME File System Integrity Value

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

5.13 - Network Stack Configuration



5.13.1 - Network Stack

Use this item to enable or disable UEFI Network Stack.

5.13.2 - Ipv4 PXE Support

Use this item to enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

5.13.3 - Ipv4 HTTP Support

Use this item to enable or disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

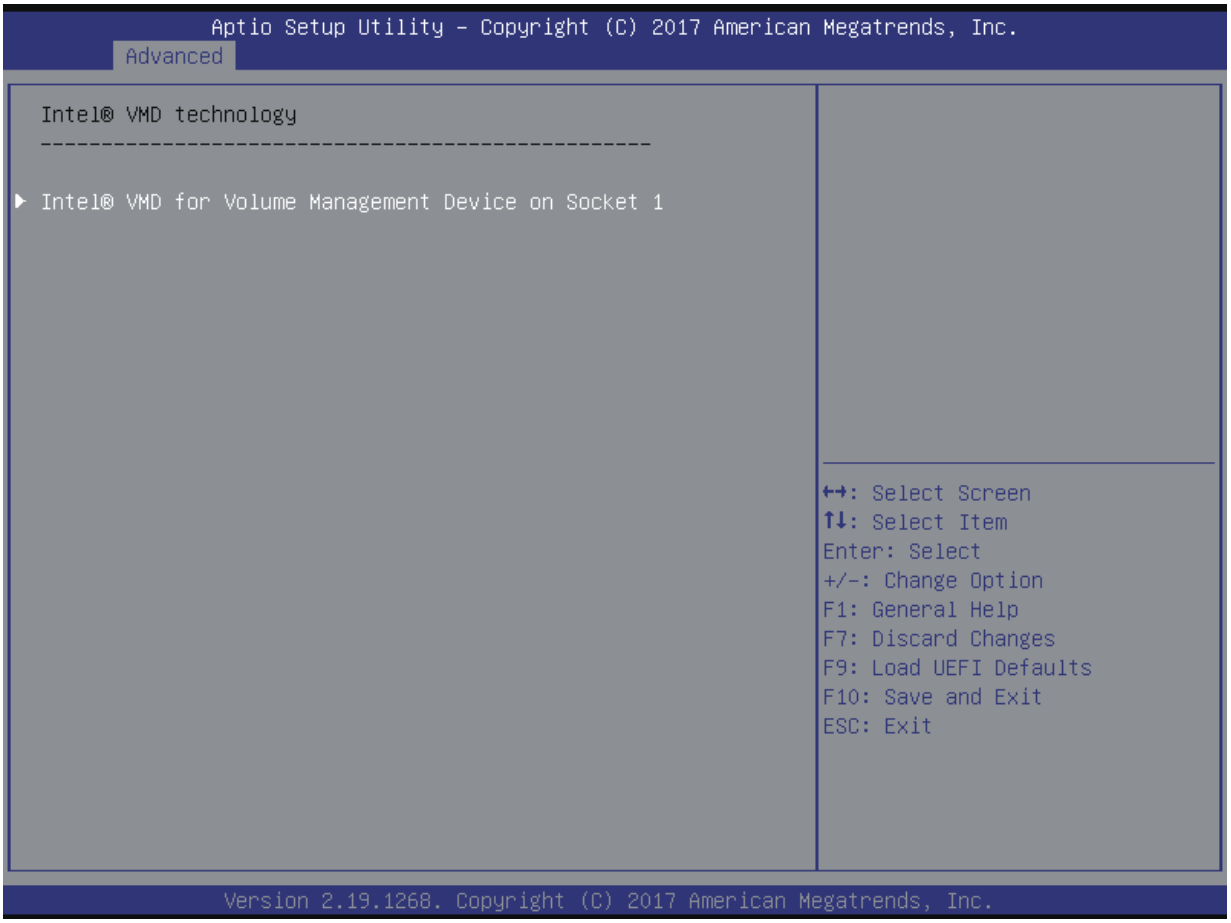
5.13.4 - Ipv6 PXE Support

Use this item to enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

5.13.5 - Ipv6 HTTP Support

Use this item to enable or disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.

5.14 - VMD Configuration



5.14.1 - Enable VMD Controller

Use this item to enable or disable the VMD Controller. When enabled, the options below appear.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

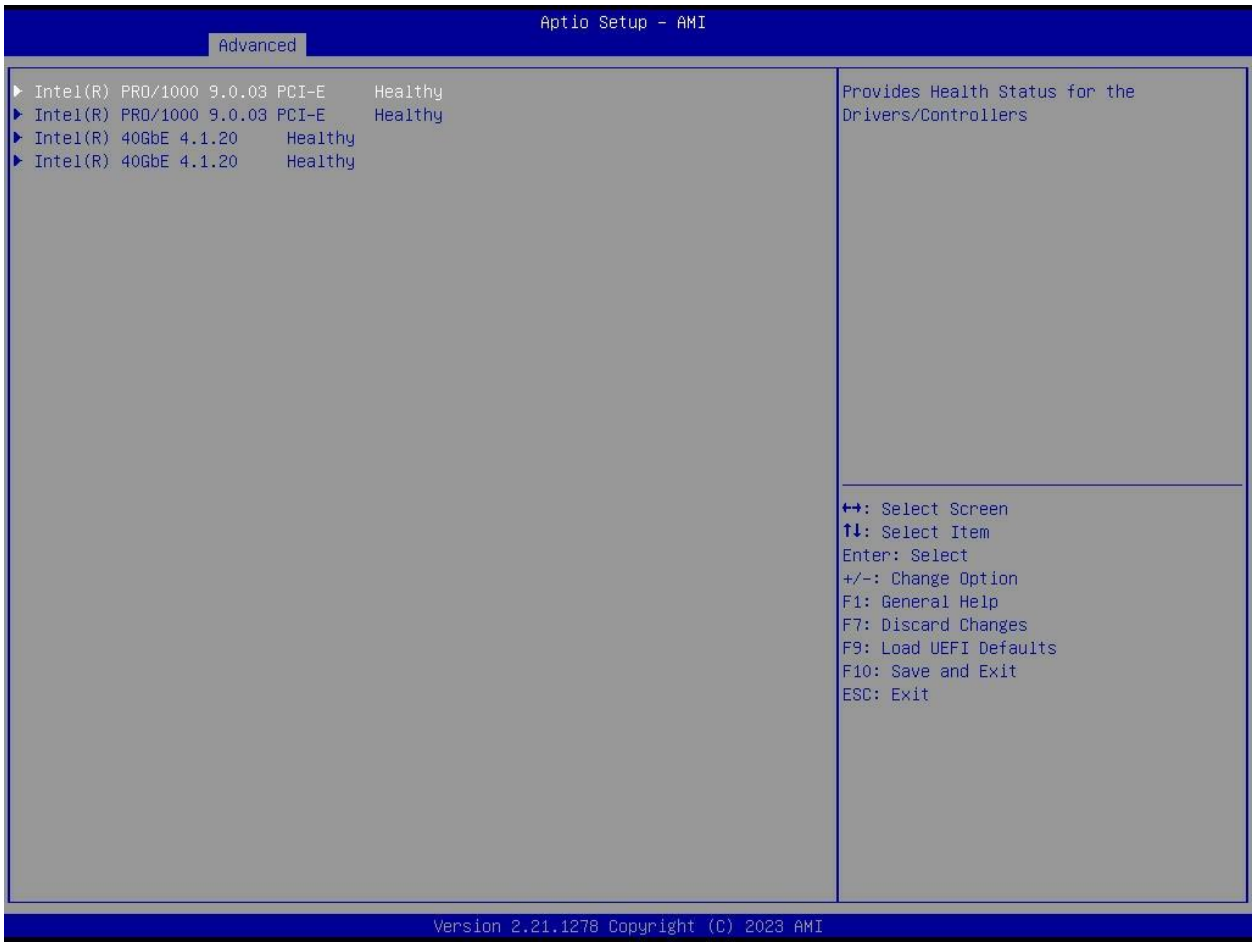
5.14.2 - Enable VMD Global Mapping

Use this item to enable or disable VMD Global Mapping.

5.14.3 - Map this Root Port under VMD

Use this item to map or unmap Root Port to VMD

5.15 - Driver Health



Provides health status for the drivers/controllers.

5.16 - Instant Flash

Instant Flash is a UEFI flash utility embedded in Flash ROM.

This utility enables UEFI firmware updates without entering operating systems.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

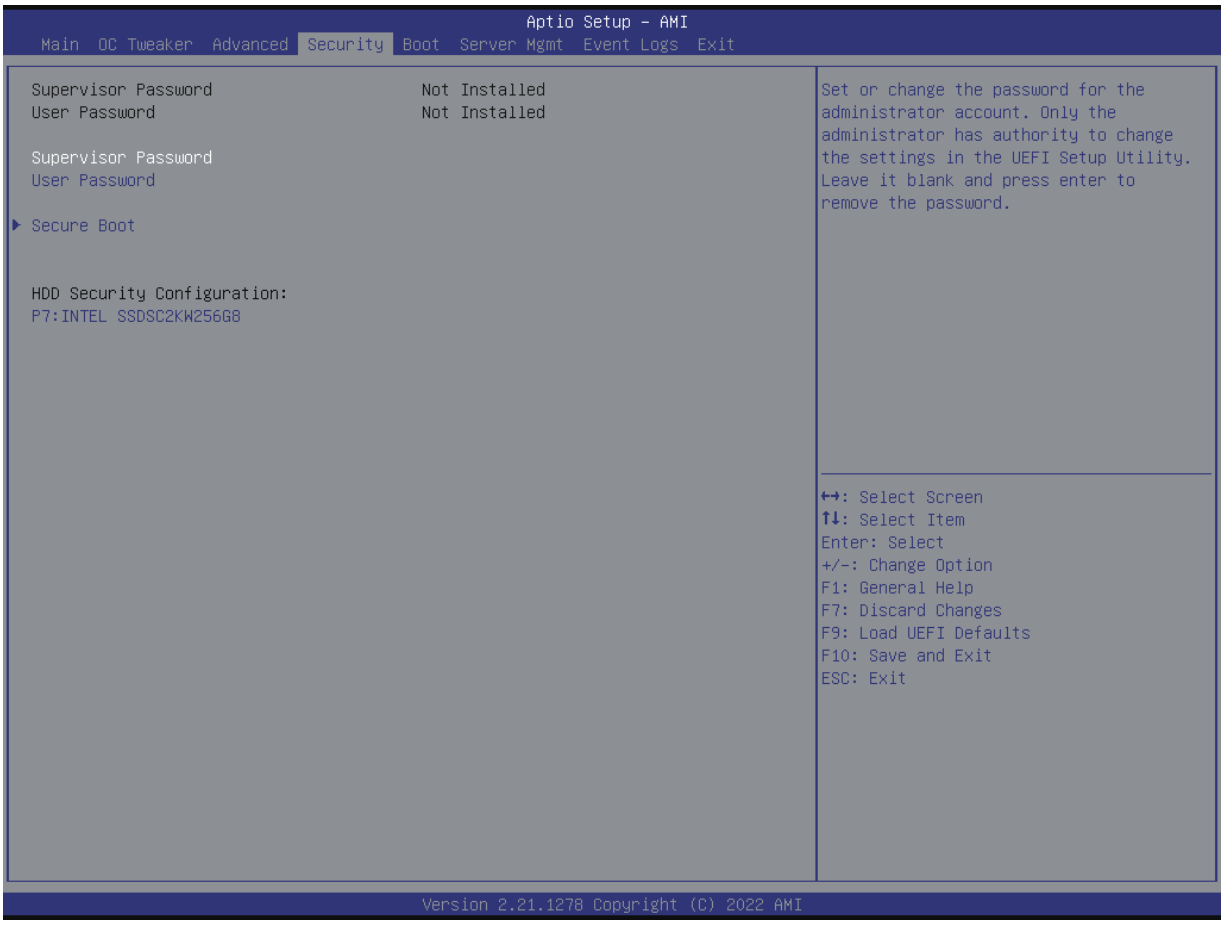
To flash UEFI firmware, download and save the new firmware version to bootable USB flash media. Then, using Instant Flash, you can update system firmware directly via Instant Flash menus through the UEFI Menu.

Please be noted that the USB flash media must use a FAT32/16/12 file system.

When the Instant Flash utility is executed, the utility will show the firmware files on the USB media and their respective information. Select the proper firmware file to update your UEFI, and reboot your system after the UEFI update process is completed.

6.0 - Security Screen

From this screen, a user may set or change the supervisor/user password for the system. You may also clear the user password.



Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

6.1 - Supervisor Password

Set or change the password for the administrator account. Only the administrator has authority to change the settings in the UEFI Setup Utility. Leave it blank and press enter to remove the password.

6.2 - User Password

Set or change the password for the user account. Users are unable to change the settings in the UEFI Setup Utility. Leave it blank and press enter to remove the password.

6.3 - Secure Boot

Use this item to enter the Secure Boot configuration page.

6.3.1 - Secure Boot

Use this item to enable or disable support for Secure Boot.

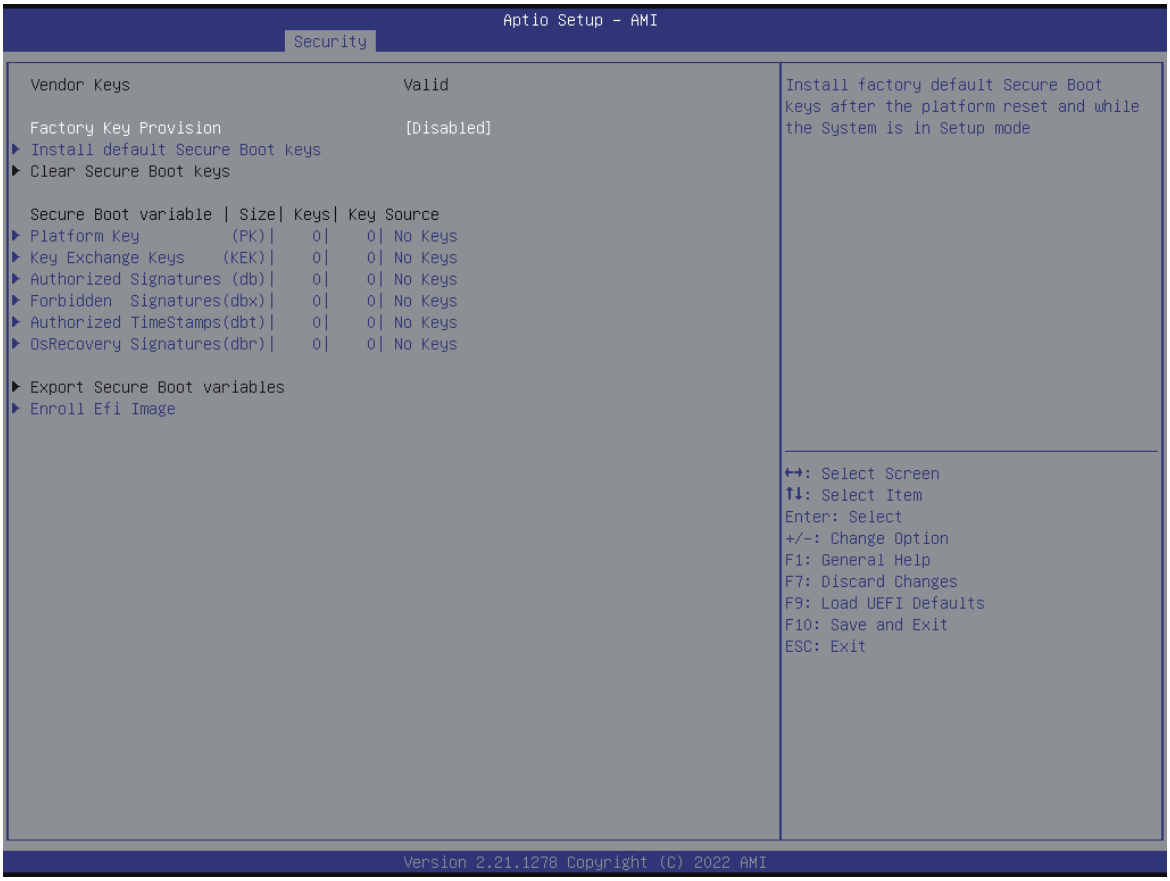
6.3.2 - Secure Boot Mode

Enable to support Windows 8 or later versions Secure Boot.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

6.3.2 - Key Management

Expert users can modify Secure Boot Policy variables without full authentication.



6.3.2.1 - Factory Key Provision

Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode.

6.3.2.2 - Install Default Secure Boot Keys

Please install default secure boot keys if it's the first time you use secure boot.

6.3.2.3 - Clear Secure Boot keys

Force System to Setup Mode - clear all Secure Boot Variables. Change takes effect after reboot.

6.3.2.4 - Export Secure Boot variables

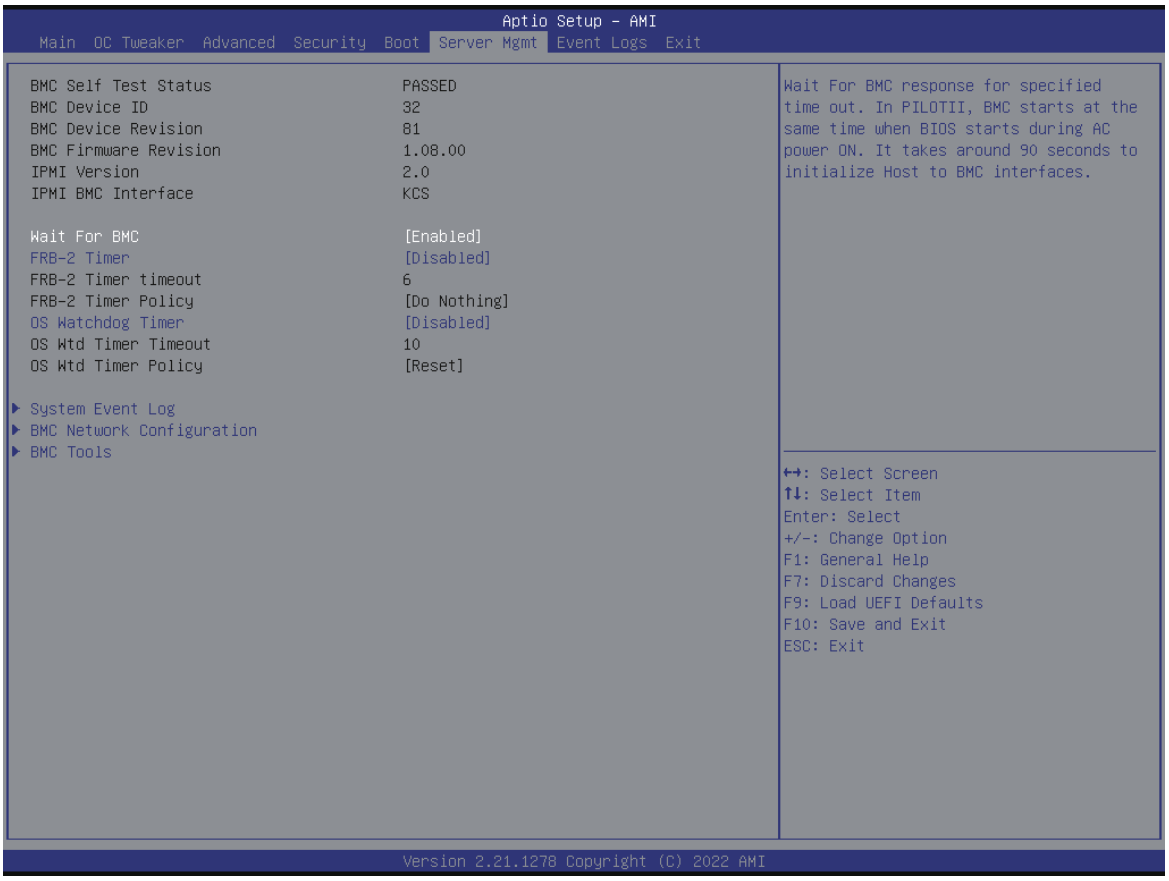
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

6.3.2.5 - Enroll Efi Image

Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db).

7.0 - Server Mgmt



7.1 - Wait For BMC

Wait For BMC response for specified time out. In PILOTII, BMC starts at the same time when BIOS starts during AC power ON. It takes around 90 seconds to initialize Host to BMC interfaces.

7.2 - FRB-2 Timer

Use this item to enable or disable FRB-2 timer (POST timer).

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

7.3 - FRB-2 Timer Timeout

Enter value between 1 to 30 min for FRB-2 Timer Expiration.

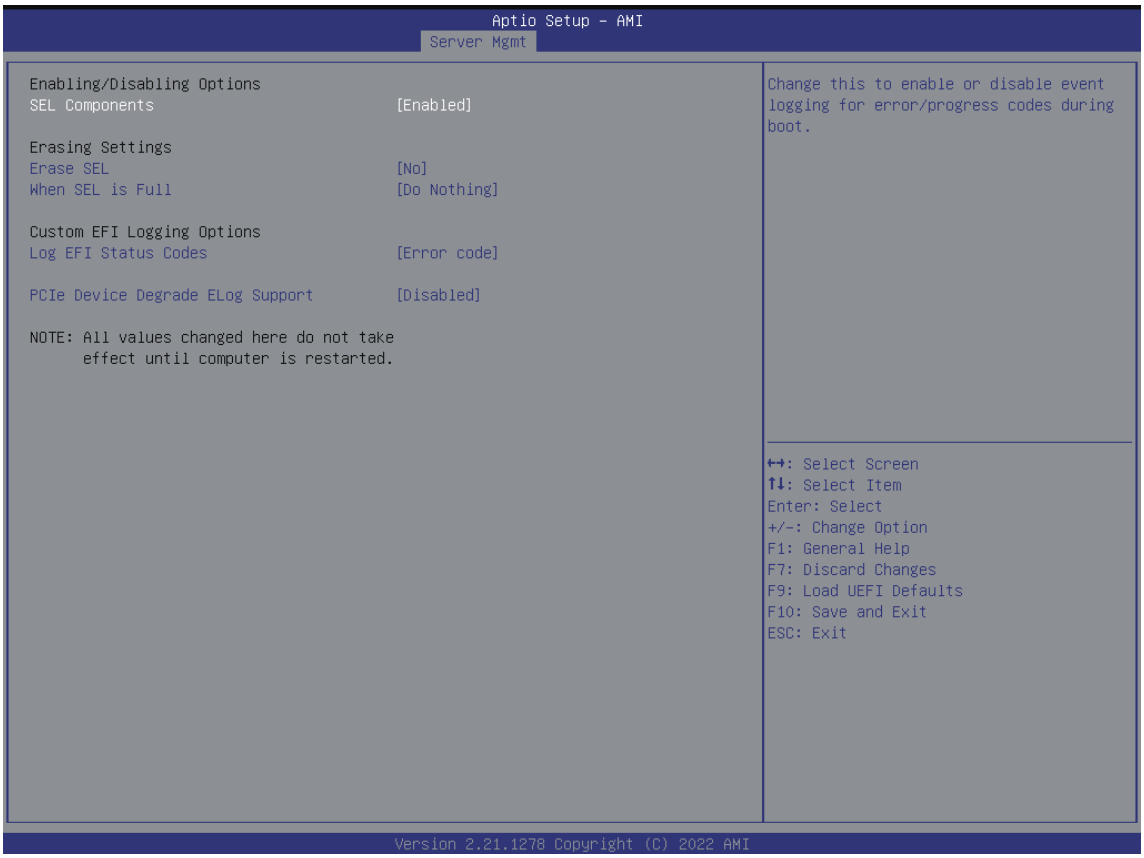
7.4 - FRB-2 Timer Policy

Use this item to configure how the system should respond if the FRB-2 Timer expires. Not available if FRB-2 Timer is disabled.

7.5 - OS Watchdog Timer

If enabled, starts a BIOS timer which can only be shut off by Management Software after the OS loads. Helps determine that the OS successfully loaded or follows the OS Boot Watchdog Timer policy.

7.6 - System Event Log



Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

7.6.1 - SEL Components

Change this to enable to disable all features of System Event Logging during boot.

7.6.2 - Erase SEL

Use this to choose options for erasing SEL.

7.6.3 - When SEL is Full

Use this to choose options for reactions to a full SEL.

7.6.4 - Log EFI Status Codes

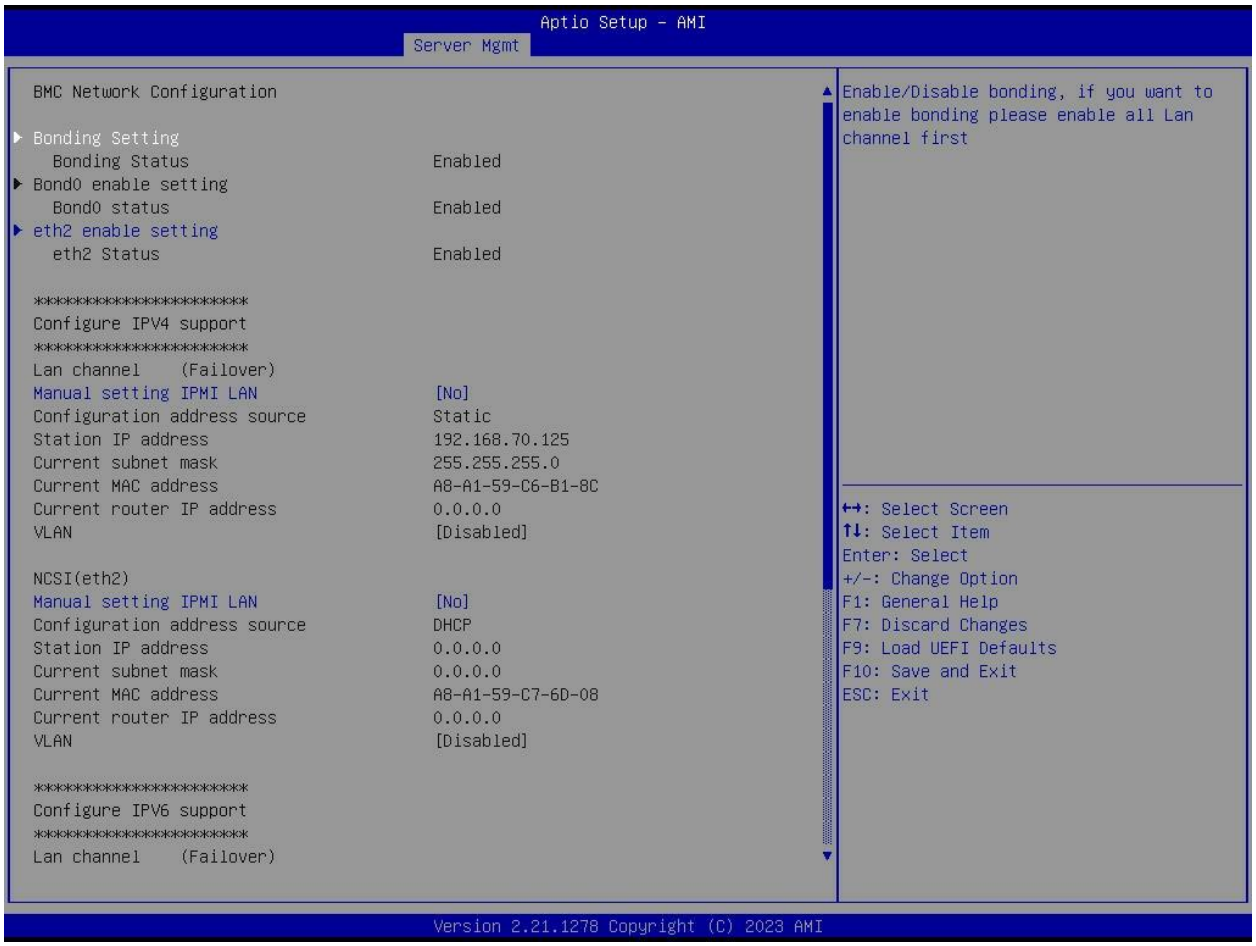
Use this item to disable the logging of EFI Status Codes or log only error code or only progress or both.

7.6.5 - PCIe Device Degrade ELog Support

Use this item to enable or disable PCIe Device Degrade Error Logging Support.

7.7 - BMC Network Configuration

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.



7.7.1 - BMC Out of Band Access

Use this item to enable or disable BMC Out of Band Access.

7.7.2 - Manual Setting IPMI LAN

If [No] is selected, the IP address is assigned by DHCP. If you prefer using a static IP address, toggle to [Yes], and the changes take effect after the system reboots. The default value is [No].

7.7.3 - Configuration Address Source

Select to configure BMC network parameters statically or dynamically(by BIOS or BMC). Configuration options: [Static] and [DHCP].

7.7.3.1 - Static

Manually enter the IP Address, Subnet Mask and Gateway Address in the BIOS for BMC LAN channel configuration.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

7.7.3.2 - DHCP

IP address, Subnet Mask and Gateway Address are automatically assigned by the network's DHCP server.

7.7.3.3 - VLAN

Enabled/Disabled Virtual Local Area Network.

If [Enabled] is selected, configure the items below.

7.7.3.4 - IPV6 Support

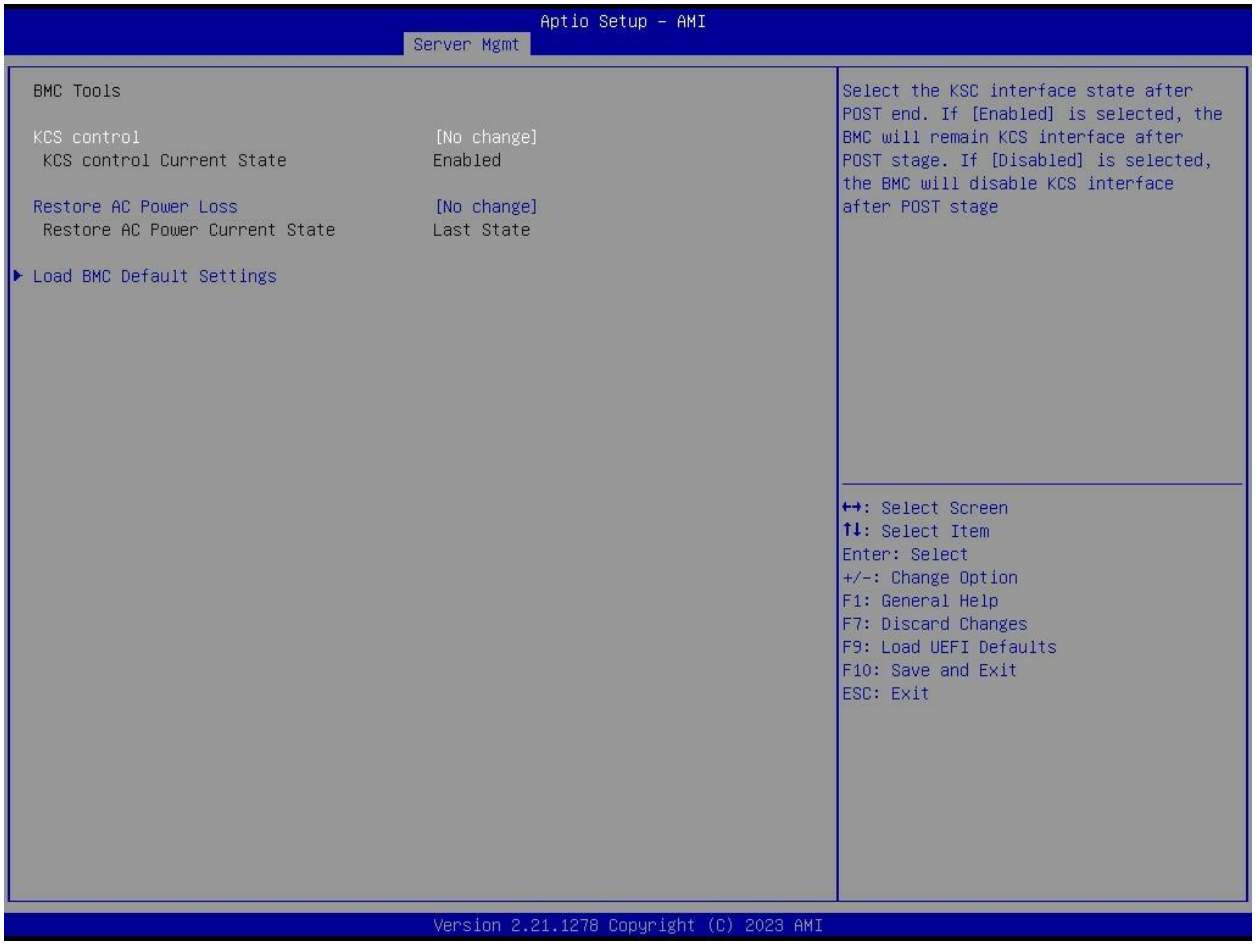
Enabled/Disable LAN1 IPV6 Support.

7.7.3.5 - Manual Setting IPMI LAN(IPV6)

Select to configure LAN channel parameters statically or dynamically(by BIOS or BMC). Unspecified option will not modify any BMC network parameters during the BIOS phase.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

7.8 - BMC Tools



7.8.1 - KCS Control

Select this KCS interface state after POST end. If [Enabled] us selected, the BMC will remain KCS interface after POST stage. If [Disabled] is selected, the BMC will disable KCS interface after POST stage

7.8.2 - Restore AC Power Loss

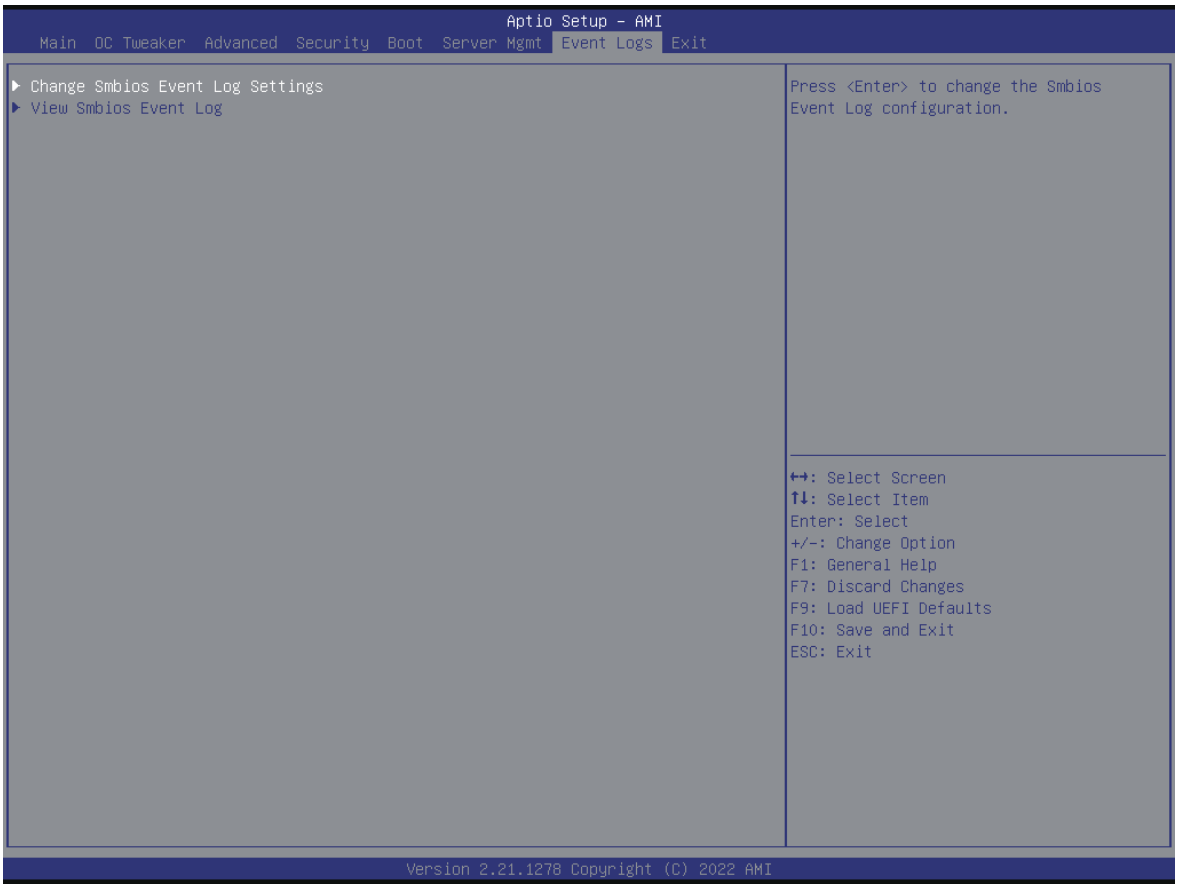
This allows you to set the power state after an unexpected AC/power loss. If [Power Off] is selected, the AC/power remains off when the power recovers. If [Power On] is selected, the AC/power resumes and the system starts to boot up when the power recovers. If [Last State] is selected, it will recover to the state before AC/power loss.

7.8.3 - Load BMC Default Settings

Use this item to Load BMC Default Settings

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

8.0 - Event Logs



8.1 - Change Smbios Event Log Settings

This allows you to configure the Smbios Event Log Settings.

When entering the item, you will see the followings:

8.1.1 - Smbios Event Log

Use this item to enable or disable all features of the SMBIOS Event Logging during system boot.

8.1.2 - Erase Event Log

The options include [No], [Yes, Next reset] and [Yes, Every reset]. If Yes is selected, all logged events will be erased.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

8.1.3 - When Log is Full

Use this item to choose options for reactions to a full Smbios Event Log. The options include [Do Nothing] and [Erase Immediately].

8.1.4 - Log System Boot Event

Choose option to enable/disable logging of System boot event.

8.1.5 - MECI (Multiple Event Count Increment)

Use this item to enter the increment value for the multiple event counter. The valid range is from 1 to 255.

8.1.6 - METW (Multiple Event Time Window)

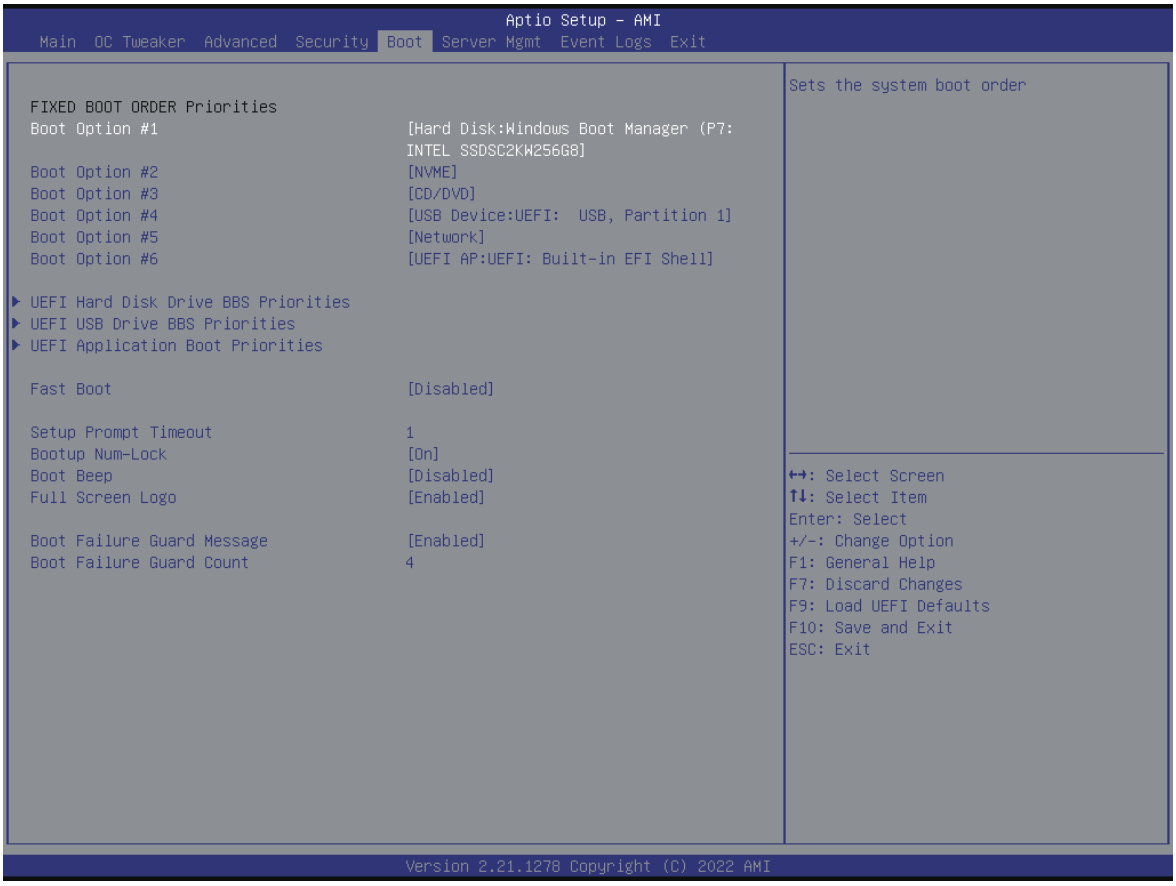
Use this item to specify the number of minutes which must pass between duplicate log entries which utilize a multiple-event counter. The value ranges from 0 to 99 minutes.

8.2 - View Smbios Event Log

Press <Enter> to view the Smbios Event Log records.

9.0 - Boot Screen

Display the available boot devices, configuration settings, and boot priority.



9.1 - Boot Option #1~#5

Use this item to set the system boot order.

9.2 - UEFI Hard Disk Drive BBS Priorities

Specifies the Boot Device Priority sequence from available UEFI Hard Disk Drives.

9.3 - UEFI USB Drive BBS Priorities

Specifies the Boot Device Priority sequence from available UEFI USB Drives.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

9.4 - UEFI Application Boot Priorities

Specifies the Boot Device Priority sequence from available UEFI Application.

9.5 - Fast Boot

Fast Boot minimizes your computer's boot time. In fast mode you may not boot from an USB storage device. Ultra Fast mode is only supported by Windows and the VBIOS must support UEFI GOP if you are using an external graphics card. Please notice that Ultra Fast mode will boot so fast that the only way to enter the UEFI System Setup Utility is to Clear CMOS or run the Restart to UEFI utility in Windows.

9.6 - Setup Prompt Timeout

Configure the number of seconds to wait for the UEFI setup utility.

9.7 - Bootup Num-Lock

If this item is set to [On], it will automatically activate the Numeric Lock function after boot-up.

9.8 - Boot Beep

Select whether the Boot Beep should be turned on or off when the system boots up.

9.9 - Full Screen Logo

Use this item to enable or disable OEM Logo. The default value is [Enabled].

9.10 - Boot Failure Guard Message

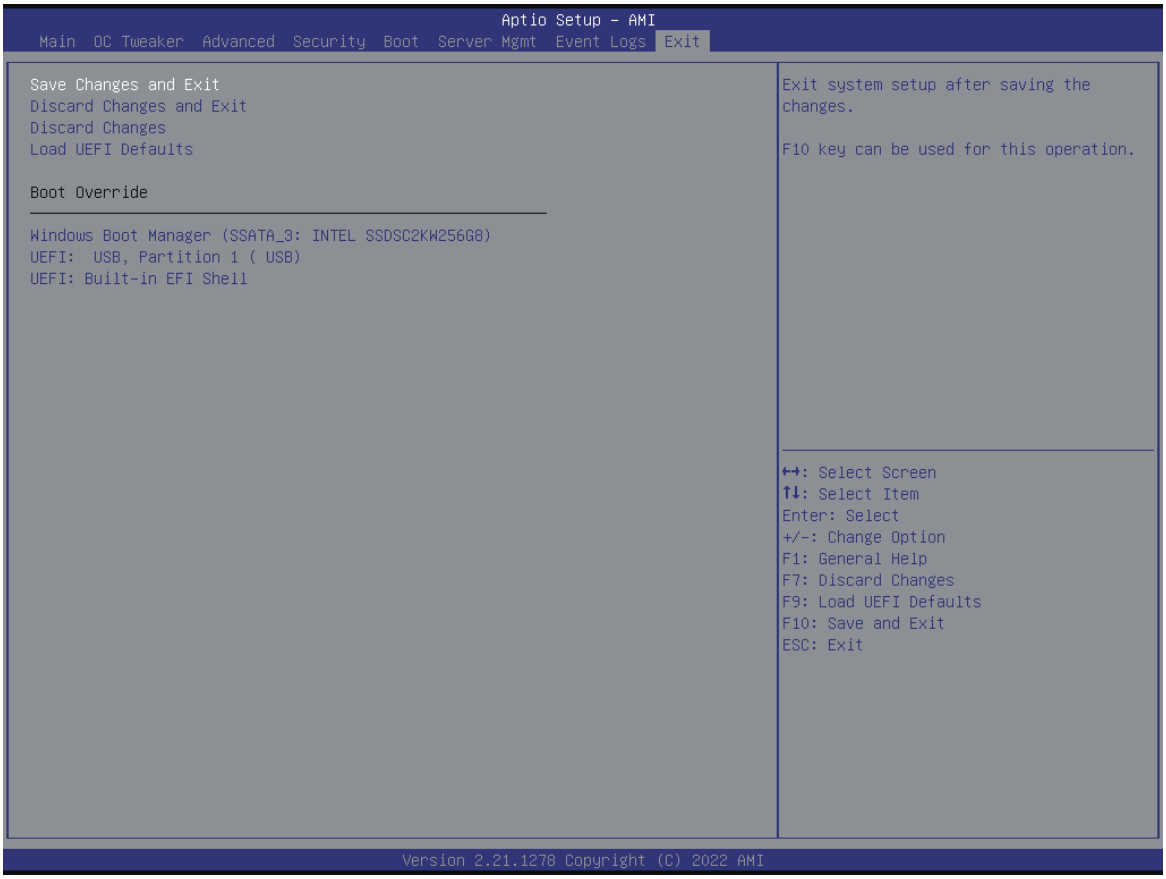
If the computer fails to boot for a number of times the system automatically restores the default settings.

9.11 - Boot Failure Guard Count

Use this item to configure Boot Failure Guard Count.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

10.0 - Exit Screen



10.1 - Save Changes and Exit

When you select this option, the following message “Save configuration changes and exit setup?” will pop-out. Press <F10> key or select [Yes] to save the changes and exit the UEFI SETUP UTILITY.

10.2 - Discard Changes and Exit

When you select this option, the following message “Discard changes and exit setup?” will pop-out. Press <ESC> key or select [Yes] to exit the UEFI SETUP UTILITY without saving any changes.

10.3 - Discard Changes

When you select this option, the following message “Discard changes?” will pop-out. Press <F7> key or select [Yes] to discard all changes.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

10.4 - Load UEFI Defaults

Load UEFI default values for all the setup questions. F9 key can be used for this operation.

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.

End of document

Note: Actual descriptive text may vary in UEFI menus. Screenshots as they appear in this user manual are for references only. Actual images may vary depending on firmware version.